Interdependencies of Degradation Effects and their Impact on Computing

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***Abstract*—Transistor degradation like aging, variability, etc. is known for a long time and some of the effects have even been discovered more than a century ago. Nevertheless, it was only around a decade ago when degradation effects became relevant within the reliability and lifetime of circuits since feature sizes of transistors began to approach atomic levels. But still in its infancy is research that investigates the *interdependencies* of these and other degradation effects. Since the causes are of physical origin, it cannot be excluded that degradation effects influence each other i.e amplify or delete each other – at least to some degree – and hence degradation effects should *jointly* and not separately be investigated. In this work, we are reporting that there are indeed interdependencies of degradation effects that are non-negligible. We quantify for the first time the interdependencies and draw their impact on computing.**

***Keywords*—BTI, RTN, HCI, RDF, Soft Errors, Aging, Reliability, Interdependencies, Guardband**

Download Software: This work is publicly available at http://ces.itec.kit.edu/dependable-hardware.php

I. Introduction

Although technology scaling enables the design of more powerful on-chip systems, designers must face the inevitable challenge regarding the fact that their circuits may not function as intended due to a wide range of degradation effects that take place during lifetime and even from the very first moment.
The key degradation effects threaten to erode reliability are:
1) Time-dependent Degradation Effects: They are due to aging phenomena that gradually shift the electrical characteristics of transistors and cause unreliable behavior.
2) Time-independent Degradation Effects: They are due to manufacturing variability that causes fluctuations in the geometry and electrical characteristics of transistors. In addition, intrinsic and extrinsic noise cause unpredictable current and voltage fluctuations that suddenly degrade the reliability.

To overcome degradation effects, chip designers continue to increase the so-called *guardband* (i.e. safety margin) of supply voltage (V_{dd}) akin to its essential role in defining the circuits' resiliency against failures. This trend is unsustainable as it counteracts with the goal to reduce V_{dd} as it is responsible for the unsustainable on-chip power densities that lead to elevated temperatures. High temperature, in turn, amplifies aging phenomena [2] and also makes circuits less resilient which compensates the reliability increase attained from the higher V_{dd} as Fig. 1 demonstrates. Moreover, unsustainable power densities enforce the so-called Dark Silicon problem [5] in which *only a subset* of processing cores within an on-chip system may operate at full performance at the same time.

While at the first glance the aforementioned degradation effects may look unrelated to each other and therefore one may separately investigate them, they are actually not due to the *interdependencies* that impose a *joint* consideration.

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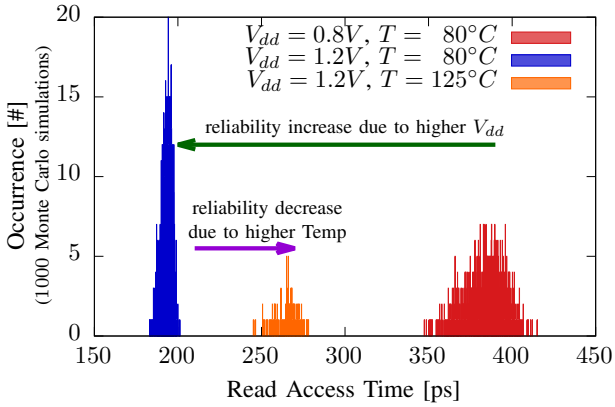

Fig. 1. Though a higher V_{dd} increases SRAMs resiliency against timing-violation failures, it concurrently leads to a higher temperature which, in turn, reduces the resiliency and thus it compensates the achieved reliability increase. SPICE simulations (based on the BSIMv4.8 [15] along with PTM [16]) of 6T SRAM cells at the 22 nm technology node.

More importantly, to answer the critical question, *"What is an efficient (i.e. sufficiently-dimensioned) guardband?"* one needs to be able to *accurately estimate* reliability with respect to diverse degradation effects – that, as mentioned, potentially influence each other. As we will demonstrate, interdependencies of degradation effects do matter for designing efficient guardbands and hence we can draw its impacts on computing.

II. Challenges in Modeling Interdependencies

Aging [6], [7], manufacturing variability [9] and noise [10], [11] have been extensively studied in state-of-the-art. However, state-of-the-art approaches often consider the respective degradation effects separately. A few works aimed to jointly consider multiple degradation effects at either the circuit level through failure-equivalent circuits or at the system level through the sum-of-failure-rates (SOFR) rule. Importantly, such a superposition has always been applied under the assumption that the considered degradation effects are independent. The reason behind why state-of-the-art models degradation effects at high abstraction levels is the sake of avoiding the complexity that comes at the physical level. While, on the one hand, this might be sufficient to provide a rough reliability estimation for quick design-time decisions, it is, on the other hand, insufficient to design efficient guardbands.
In fact, these degradation effects share several common parameters because their causes are of physical origin and therefore they are *interdependent* from a physical point of view. Neglecting interdependencies leads to inaccurately estimating the joint impact of degradation effects due to the high degree

of uncertainty – as they may indeed amplify or mitigate each other over time. Such inaccuracy makes chips designers be conservative and thus design non-efficient guardbands.

The first attempt towards considering interdependencies, at the physical level, has recently been presented in [1], where we found that non-accounting for the interdependencies of BTI and HCID aging phenomena does in fact result in a non-negligible underestimation of the allover reliability. Physics-based models are more accurate, contrary to higher-level models, but complex [1] as they aim to describe in-depth the underlying chemical mechanisms that occur over time within the dielectric of a single transistor (e.g., mechanisms of breaking and annealing Si-H bonds [6]). Therefore, such sophisticated modeling may not be feasible for system-level designers who deal with estimating the reliability of an on-chip system – consisting of an enormous number of transistors – during its entire lifetime (e.g., years). To address this challenge, we presented in [2] an approach that provides significant speedups through exploiting the physical properties of degradation effects along with building an FPGA-based platform emulator.

Our novel contributions within this article:

1) We expand our focus from solely investigating aging phenomena – as it was in [1], [2] – towards additionally investigating diverse degradation effects from other domains through: a) considering the effects of the fluctuations in transistors characteristics due to manufacturing variability and b) considering the effects of intrinsic and extrinsic noise.
2) We present, in this work, how diverse degradation effects induced by aging, variability and noise can properly be combined at the physical level towards providing designers, at system-level, with an accurate reliability estimation in the scope of existing interdependencies.
3) We evaluate the impact of interdependencies on computing to show that they do matter, not solely at the physical level, but also at the system level and hence the joint consideration is indispensable when an efficient guardband is required.

III. Degradation Effects with Interdependencies

Unlike the effects of aging that manifest themselves over time as shifts in the transistors electrical characteristics (i.e, voltage threshold V_{TH} and carrier mobility μ), manufacturing variability causes, from the initial state (i.e. before operation), the electrical characteristics of transistors to follow statistical distributions due to the fluctuations in both transistor geometry (i.e. length L and width W) and V_{TH}.

In addition, effects of noise – either intrinsic due to the activities within the chip itself or extrinsic due to radiation (i.e. external energetic particles) – are able to cause a sudden change in the V_{TH} of transistors at a random point of time.

Why Guardband? The overall impact of these diverse degradation effects can be expressed through the transistor drain current (I_D) as Fig. 2 clarifies. To compensate degradation effects, designers apply a guardband G on top of V_{dd} to ensure that the operational I_D will always be as intended and thus the reliability will constantly be sustained during lifetime. Guardbands may also be employed with respect to transistors characteristics (e.g., increasing the width of transistors and/or the dopant concentration). However, this necessitates turning manufacturing. Importantly, transistors characteristics are fixed after manufacturing. By contrast, V_{dd} can be changed during runtime and hence we focus on it. However, safe V_{dd} transitions (i.e. without transient errors), necessitate taking aging into account, for example by employing our A-GEAR technique presented in [3].

A. Effects of Aging

With technology in the nano-CMOS era, the susceptibility of transistors to the following aging phenomena[1] is increasing:

Bias Temperature Instability (BTI): It is caused by the trap generation in the $Si\text{-}SiO_2$ interface of a transistor (i.e. interface traps) as well as deep within the transistor dielectric (i.e. oxide traps).

Hot Carrier-Induced Degradation (HCID): It is caused by *hot carriers* within the channel of transistor where their kinetic energy is sufficient to form electron-hole pairs. In contrast to BTI, HCID generates only interface traps.

During lifetime, interface and oxide traps cause charge buildup and thus they manifest themselves as shift in the V_{TH}. Additionally, carriers mobility μ also degrades but due to interface traps solely as oxide traps locate deep within the dielectric (i.e. they cannot interact with carriers inside the channel). In this work, we rely on our aging modeling in [1] where the joint effect of BTI and HCID on V_{TH} and μ has been modeled at the physical level through the generated traps. Based on the estimated degradations, we directly change V_{TH} and μ in the transistor parameters within the PTM [16]. This ensures considering the consequences of these degradations in all internal calculations of BSIM [15], in which the electrical characteristics of nMOS/pMOS are modeled.

B. Effects of Manufacturing Variability

Process variation (PV): It is due to the geometric variance during IC fabrication as lithography techniques reach their resolution limits. PV is typically modeled as a normal distribution for W and L of a transistor.

Random Dopant Fluctuation (RDF): It is due to the fluctuations in the dopant concentration which can ease or hinder the channel formation during operation. Therefore, RDF directly influences the V_{TH} of a transistor [9] and such an impact is also modeled as a normal distribution [9]. To consider the effects of both PV and RDF on the transistor characteristics, Monte Carlo simulations based on the corresponding normal distributions can be employed. Note that the deviations from the nominal W, L and V_{TH} due to PV and PDF consequently fluctuate the drain current of transistor (I_D) (see Eq. 1).

C. Effects of Noise

The degradations in the transistor characteristics reduce the resiliency of circuits against noise, that may unpredictably change the specified behavior of circuits and thus cause failures. Therefore, accurately estimating the reliability necessitates taking also noise effects into consideration to quantify interference. Noise may be intrinsic or extrinsic and the effects of both can be modeled as a function of V_{TH}.

Intrinsic Noise: Within a transistor a couple of traditional

[1] Aging in interconnects, e.g. electro-migration, is not considered here as it is independent to other degradations that occur jointly inside the transistor.

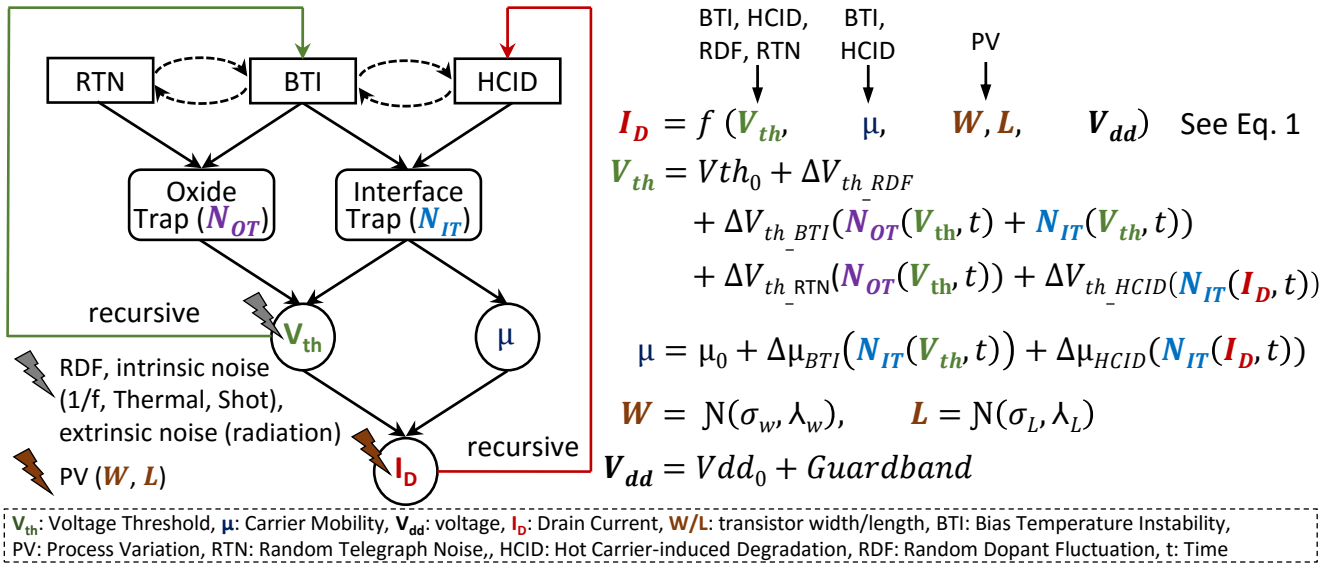

Fig. 2. Interdependencies of degradation effects (left) and how the joint impact of them is represented through the drain current (I_D) of transistor (right).

noise kinds may occur: Shot noise, 1/f noise and thermal noise. In contrast to them, Random Telegraph Noise (RTN) became more apparent due to the critical shrinking in feature sizes. It is a noise effect, within the transistor dielectric, which manifests itself as discrete random jumps in V_{TH} due to the capture/emission of charges in potential oxide traps [11].

In practice, we employ, on the one hand, the BSIM modeling from Berkeley to model the traditional noise kinds (i.e. thermal, shot and 1/f noise) as it has been established to be well suited [12] and it is also able to provide us with the V_{noise}, i.e. $V_{TH}(Noise)$. On the other hand, we employ the presented modeling in [10], [11] to consider the effects of RTN as it describes the RTN impact on V_{TH} through the stochastic capturing/releasing of charges in traps.

Extrinsic Noise: Strikes by particles (e.g. neutrons) manifest themselves as an extrinsic noise to circuits which may transiently disrupt the logical state of transistors.

The effect of a particle strike is modeled through the exponential current flow based on the rise/fall time and deposited charges as demonstrated in [13]. By iterative SPICE simulations, the minimal current which is able to disrupt the logical state at the strike position can be determined. By employing a guardband that tolerates such a current, a particle needs to deposit at least double of that current to disrupt the logical state. This is very unlikely as deposited charges of particle strikes follow an exponential distribution [17].

Last but not least, the effects of aging (on V_{TH} and μ), manufacturing variability (on L, W and V_{TH}) and noise (on V_{TH}) are jointly represented within the drain current (I_D) model of MOSFET as it is a function of all of them. Fig. 2 demonstrates the interdependencies of degradation effects along with the role I_D. The latter is clarified through the first order approximation in the following equation.

$$I_D \approx \frac{\mu}{2} \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{dd} - V_{th})^2 \quad (1)$$

D. Putting it all together: Aging, Variability and Noise

We showed in [1] the existing interdependencies of BTI and HCID aging phenomena as they share one kind of defects (i.e. interface traps N_{IT}). Due to the common defects, BTI over time influences the physical cause of HCID and vice versa [1], [7]. The rate of defect generation and recovery due to BTI and HCID recursively depends on V_{th} and I_D, respectively, as presented models in [1] establish. Importantly, due to the recursive dependency, manufacturing variability is able to influence aging effects as it results in fluctuations in both V_{th} and I_D (see Section III-B). Furthermore, interdependencies of BTI and RTN also occur, over time, as they both share the same kind of defects (i.e. oxide traps N_{OT}). In fact, the magnitude of RTN, at any point of time, is defined based on the generation of oxide traps which is *driven* by BTI [8]. Therefore, BTI, HCID and RTN effects influence each other and, additionally, one must consider them in the scope of PV and RDF effects. Fig. 2 demonstrates the studied degradation effects along with the interdependencies of them.

In order to maintain a proper *joint* consideration of the studied degeneration effects, we selected the employed models in Section (III-A, III-B and III-C) to ensure that the physical interdependencies (i.e. the common parameters among degradation effects) are represented.

At foremost, the employed physical models describe BTI, HCID and RTN through the generated defects (i.e. interface N_{IT} and oxide N_{OT} traps) and thus they enable us to capture the interdependencies of BTI and HCID (that are caused by interface traps) as well as the interdependencies of BTI and RTN (that are caused by oxide traps). Then, modeling the effects of BTI, HCID and RTN through V_{th} enables us to capture the effects of RDF and noise (shot, 1/f, thermal noise and radiation). Furthermore, considering the I_D modeling enables us to additionally capture the effects of BTI and HCID on μ and the effects of PV on W and L of transistors.

Finally, modeling all degradation effects through a common metric (I_D) (see Fig. 2) along with the recursive dependencies (see Fig. 2 (left)) provides us with the *joint* overall impact of aging, variability and noise in the scope of the interdependencies towards accurately estimating reliability and designing an efficient guardband (G) which is the focus of this work.

E. Bringing Temperature into Play

As a matter of fact, temperature is one of the pivotal parameters when it comes to reliability. It plays a fundamental role in defining the strength of degradation effects as it strongly influences the electrical characteristics of transistors (e.g, V_{th}, μ, etc.) [15]. On-chip temperatures are *driven* by the running workloads. Therefore, we employ the gem5 simulator for the Alpha architecture to extract the activities of various applications. Afterwards, we estimate the static/dynamic power consumption by the McPAT tool. Based on the resulting power densities, the thermal simulator HotSpot provides us with the corresponding thermal maps of CPU. Further details regarding the developed framework to estimate the temperature are presented in [2]. Then, the effects of temperature on transistors are taken into account through the MOSFET modeling from Berkeley (BSIM) [15]. This allows us to consider the impact of temperature on the studied degradation effects.

Aging: High temperatures amplify aging effects [1]. In addition, aging (e.g., BTI) increases the gate leakage (due to the oxide traps) and thus it leads over time to a higher temperature due to the higher static power consumption [6].

Manufacturing Variability: It modulates (i.e. randomly increases or decreases) the on-chip power densities and thus the operating temperatures due to the fluctuations in gate and subthreshold leakage power [9].

Noise: An increase in temperature leads to higher noise amplitudes due to amplifying the physical causes behind noise. The susceptibility to radiation increases with higher temperatures because higher temperatures result in smaller critical charge (Q_{crit}) which is the minimum amount of charges to cause a soft error. This may make the deposited charges due to even neutrons, which are abundantly available at the sea level, become sufficient to provoke soft errors in memory cells.

IV. Impact of Interdependencies on Computing

Interdependencies of degradation effects influence computing in various ways. The most pronounced are: a) considering interdependencies has the potential to designing more efficient guardbands due to the higher certainty coming from estimating the reliability more accurately. b) neglecting interdependencies leads to wrong principles when it comes to mitigation (i.e. reliability-increase) techniques. In other words, considering interdependencies also opens the door of revisiting the current principles of mitigation techniques to ensure that they are still valid in the scope of diverse degradation effects.

A. Designing Efficient Guardbands

There is the prospect of indeed *containing* guardbands and thereby making them more *efficient*. This is against a current trend that requires *increased* guardbands with all its negative implications on power and temperature. Fig. 3(a) illustrates that a *separated* consideration of degradation effects (i.e. without paying attention to the existing interdependencies) results in designing a non-efficient (i.e. conservative) overall guardband by 17%. This is primarily because degradation effects, in reality, influence each other i.e amplify or delete each other as the causes behind them are of physical origin. To investigate why, Fig. 3(b) demonstrates, for instance, the impact of considering the interdependencies on reducing the guardband of BTI alone. Here, as soon as the interdependencies of BTI and HCID are additionally considered, the required guardband becomes 8% more efficient compared to separately considering BTI – although other interdependencies are still not included yet. Importantly, considering other interdependencies reduce the guardband further to 81%. Note that the reduction in the overall is smaller because RDF and PV are not affected by the time-dependent degradation effects. In this case study, a 22 nm PTM [16] along with BSIMv4.8 has been employed in the our joint modeling of degradation effects under the operating conditions of $T = 125°C$, $V_{dd} = 1.0V$ (details in Appendix).

Consequences of efficient guardbands: Such a reduction in the designed guardband, in practice allows for a lower operating voltage (V_{dd}) (see Fig. 2 (right)). Thus, the key properties of a processor in terms of power consumption and temperature will be influenced as both are *driven* by V_{dd}. As shown in Fig. 5, an efficient guardband – due to the joint consideration of degradation effects – results in a minimum temperature overhead (around $0.4°C$) which is 84% better compared to the case where interdependencies of degradation effects are neglected. These results have been conducted from our built platform of the Alpha processor [2] along with representative workloads of different benchmarks. The guardband can be also be effectively included intrinsically within the circuit's design through providing the synthesis tool with the required degradation information of gates [4].

B. Breaking Principles within Current Mitigation Techniques

Beside designing efficient guardbands, considering interdependencies also reveals new observations that were unseen before. Such observations may break some of the principles within current mitigation techniques, as we will demonstrate.

Soft error mitigation techniques are based on the assumption that the probability of failure across the cells of the protected memory component is identical. However, due to the interdependencies of degradation effects, similar cells become differently susceptible to radiation over time as Fig. 4-(a) shows. To be exact, activities akin to the running applications on top of the processor cause similar memory cells to differently age. Then, due to the interdependencies of aging and radiation, each memory cell will have a different critical charge. Fig. 4-(b) demonstrates how considering the interdependencies of aging and radiation makes the SRAM cells within the register file component of the LEON3 processor have different probability of failure after a lifetime of 10 years. The experimental hardware setup is discussed in detail in our previous work [2].

To the best of our knowledge, this the first time where it is investigated how interdependencies turn homogeneous structures into heterogeneous which may enforce revisiting the reliability-increase techniques to ensure they are still efficient and their principles are still valid!

V. Conclusion

Technology scaling provides, by an increased pace, designers with superior improvements but it concurrently causes on-chip systems to become thermally constrained due to the unsustainable power densities originated from the discontinuation of Dennard's scaling. The diverse degradation effects due to scaling relentlessly push the reliability to the forefront

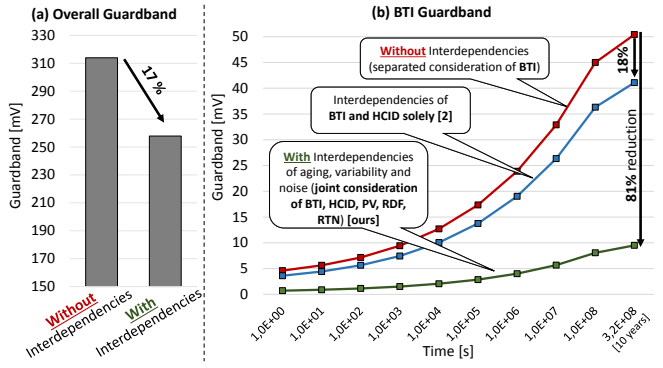

Fig. 3. Impact of interdependencies on designing guardbands to prevent I_D from dropping below its specification. (a) shows the impact on the overall guardband in the scope of all degradation effects and (b) demonstrates the impact on the guardband in the scope of BTI alone. Simulations were performed on 22nm PTM with BSIMv4.8 at ($125°C$, 1.0V). Overall guardband reduction is smaller as RDF/PV have a considerable contribution and cannot be mitigated by aging effects. In more controlled manufacturing processes (i.e. less RDF/PV) the guardband reduction becomes higher.

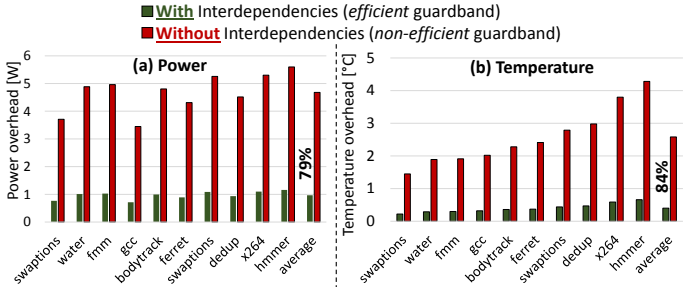

Fig. 5. Impact of designing *efficient* guardband (when interdependencies are considered) and *non-efficient* guardband (when interdependencies are neglected) on computing with respect to temperature (a) and power (b). On-chip systems in the current and upcoming technology nodes are thermally constrained. Therefore, an *efficient* guardband coming with a minimum overhead on temperature is indispensable.

and implicate increasing the V_{dd} guardband which, in turn, exacerbates the problem of unsustainable power densities.

In this article, we demonstrated for the first time that degradation effects need to be jointly investigated due to their inherent interdependencies. We then showed how considering interdependencies leads to designing an efficient guardband which, in turn, results in a considerable reduction in the temperature and power overheads of guardband. Finally, we explored how neglecting the interdependencies may also jeopardize the effectiveness of reliability-increase techniques due to breaking some of their principles.

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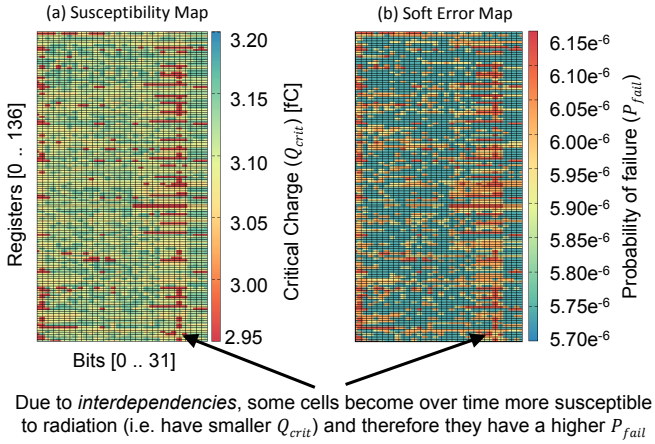

Fig. 4. Soft error analysis of the register file of the LEON3 processor while running a representative workload ("jpeg" benchmark on top of the Linux OS). The heterogeneity across the cells is due to the interdependencies of degradation (aging and radiation) effects for the lifetime of 10 years.

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VI. APPENDIX

Details of the presented equations in Fig. 2 showing the individual models that we employ to model that joint impact of degradation effects.

BTI & HCID

$$\Delta V_{th} = \frac{q}{C_{ox}} \cdot (N_{IT.BTI} + N_{IT.HCID} + N_{HT} + N_{OT})$$
$$\mu = \frac{\mu_0}{1+\alpha \cdot (N_{IT.BTI}+N_{IT.HCID})}$$

Description: Combined threshold voltage and mobility shift, due to interface and oxide traps, which originate due to BTI and HCID. For a detailed explanation refer to [1]

Interface Traps

$$N_{IT.BTI} = A(V_{GS} - V_{th} - \Delta V_{th})^{\Gamma_{IT}} e^{\frac{-E_{AIT}}{kT}} \cdot t^{n_1} d^{n_1}$$
$$d = \frac{\Lambda}{1+\sqrt{\frac{1-\Lambda}{2}}}; \; E_{AIT} = \frac{2}{3}(E_{Akf} - E_{Akr}) + \frac{E_{ADH2}}{6}$$
$$N_{IT.HCID} = B\left[t \cdot \frac{I_{DS}}{W} \cdot e^{-\frac{\Phi_{IT,e}}{q\lambda_e E_m}}\right]^{n_2}$$
$$\text{with } E_m = \frac{V_{DS}-V_{DSAT}}{\sqrt{\frac{\epsilon_{Si}}{\epsilon_{SiO_2}} \cdot t_{ox} \cdot x_j}} \text{ and } V_{DSAT} = \frac{(V_{GS}-V_{th}) \cdot L \cdot E_{cr}}{V_{GS}-V_{th}+L \cdot E_{cr}}$$

Description: Generation of interface traps (broken Si-H bounds in the gate dielectric of a transistor) due the electric field (BTI) and hot carriers (HCID). For a detailed explanation please refer to [6],[14]

Oxide Traps

Stress Phase

$$N_{HT} = C(V_{GS} - V_{th} - \Delta V_{th})^{\Gamma_{HT}} \cdot e^{\frac{-E_{AHT}}{kT}} \cdot (1 - e^{-(\frac{t}{\tau})^{\beta_{HT}}})$$
$$N_{OT} = D(1 - e^{-(\frac{t}{n})^{\beta_{OT}}})$$
$$n = \eta(V_{GS} - V_{th} - \Delta V_{th})^{-\frac{\Gamma_{OT}}{\beta_{OT}}} \cdot e^{\frac{E_{AOT}}{kT\beta_{OT}}}$$

Recovery Phase:

$$\Delta N_{HT} + \Delta N_{OT} = E(e^{-(\frac{t}{\tau_r})^{\beta_{HTR}}})$$

Description: Generation (HT) and activation (OT) of oxide traps (oxide vacancies which can be electrically activated/deactiviated with the capture/emission of a channel carrier) due the electric field (BTI) over the gate dielectric. Detailed explanation can be found in [6]

Random Dopant Fluctuation (RDF)

$$V_{th}(RDF) = \frac{1}{\sigma_{RDF}\sqrt{2\pi}} \cdot e^{-\frac{(x-\mu_{RDF})^2}{2\sigma_{RDF}^2}}$$
$$\mu_{RDF} = V_{th_{nominal}}$$
$$\sigma_{RDF} = \frac{q \cdot t_{ox}}{\epsilon_{ox}} \cdot \sqrt{\frac{N_A \cdot W_d}{4 \cdot L_{eff} \cdot W_{eff}}}$$

Description: RDF is assumed to be normal distributed with mean $_{RDF}$ and standard deviation $\sigma_{RDF} \cdot {}_{RDF}$ is nominal V_{th}. σ_{RDF} is based upon [9] and can reach 60mV.

Process Variation (PV)

$$W = \frac{1}{\sigma_{PV}\sqrt{2\pi}} \cdot e^{-\frac{(x-\mu_{PV})^2}{2\sigma_{PV}^2}}$$
$$L = \frac{1}{\sigma_{PV}\sqrt{2\pi}} \cdot e^{-\frac{(x-\mu_{PV})^2}{2\sigma_{PV}^2}}$$

Description: PV is modeled with normal distributions for the width W and length L of the transistor according to [1]

High Energy Neutrons:

$$\Delta I_D(t) = \frac{Q}{t_{fall}-t_{rise}} \cdot (e^{-\frac{t}{t_{fall}}} - e^{-\frac{t}{t_{rise}}})$$

Description: Neutron strikes are modeled with exponentially rising and falling current spikes according to [13]. Their impact is described in [1]

Random Telegragh Noise (RTN)

$$\Delta V_{th}(RTN) = X \cdot Y \text{ where}$$
$$X = \frac{1}{\sigma_{traps}\sqrt{2\pi}} \cdot e^{-\frac{(X-\mu_{traps})^2}{2 \cdot \sigma_{traps}^2}}$$
$$Y = \frac{1}{\sigma_{V_{th}}\sqrt{2\pi}} \cdot e^{-\frac{(Y-\mu_{V_{th}})^2}{2 \cdot \sigma_{V_{th}}^2}}$$

with PMOS: $\mu_{traps} = 2.7$ and $\sigma_{traps} = 2.3$

$\mu_{V_{th}} = 16.2mV$; $\sigma_{V_{th}} = 43.8mV$

and NMOS: $\mu_{traps} = 1.5$ and $\sigma_{traps} = 1.5$

$\mu_{V_{th}} = 13.8mV$; $\sigma_{V_{th}} = 37.2mV$

Description: $\Delta V_{th}(RTN)$ is modeled via probabilistic variables, which probability density functions are normal distributed. X is the number of traps, with mean μ_{traps} and standard deviation σ_{traps} [10]. Y is the ΔV_{th} per trap, with mean $\mu_{V_{th}}$ and standard deviation $\sigma_{V_{th}}$ [11].

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