

# 12TH ACM/IEEE EMBEDDED SYSTEMS WEEK



## 2016 ESWEEK PROGRAM

OCTOBER 2-7, 2016 | PITTSBURGH, PA | USA

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# WELCOME TO ESWEEK 2016



**Jörg Henkel | General Chair**  
*KIT Karlsruhe, Germany*



**Lothar Thiele | Vice-General Chair**  
*Swiss Federal Institute of Technology, Zurich, Switzerland*

## Welcome to the IEEE/ACM Embedded Systems Week 2016!

This year the embedded systems community meets in Pittsburg, following the tradition of ESWEEK to rotate between Asia, Europe and North America.

At the core of ESWEEK from Monday to Wednesday are the three conferences CASES, Codes+ISSS and EMSOFT that received 63 technical papers (acceptance ratio 29%), 80 (26%) and 98 (26%), respectively. Besides the technical paper sessions, special sessions continue to be an important part of the conferences as experts give overviews of the newest embedded systems trends.

New this year is a focus on the Internet-of-Things: The “IoT Day” (part of Codes+ISSS) will take place on Tuesday presenting newest trends in IoT as a mix of technical papers, special sessions and invited speakers from an embedded systems point of view.

For the first time, the review process of the conferences was conducted in a journal-like two-stage peer-reviewed process with the opportunity of minor/major revision before final decision. This was in an effort to further increase the high quality of ESWEEK publications. It was also an intermediate step before ESWEEK intends to move to a journal-integrated publication model in 2017 where the majority of ESWEEK papers will be published either at an ACM or IEEE journal in an alternating way year by year.

Highlights of ESWEEK are the three keynotes: The Monday keynote by Prof. Srinu Devadas from MIT will emphasize the importance of security in the age of the Internet-of-Things in “Secure Hardware Platforms for the Internet of Things (IoT)”. The Tuesday keynote by Louis K. Scheffer from the Howard Hughes Medical Institute presents new paradigms of how to design software and hardware in “Learning from Life”.

Finally, the Wednesday keynote by Kaushik Roy from Purdue University presents the newest trends in approximate computing, a new paradigm that promises to increase the computing efficiency. His talk is entitled “Approximate Computing for Energy-efficient Error-resilient Systems”.

The conference program will be concluded with the traditional panel on Wednesday afternoon focusing this year on “Embedded Systems Challenges in the Era of Cyber-Physical Systems and Internet of Things”. It will provide the opportunity to discuss CPS and IoT topics with international experts. Further highlights are the five tutorials on Sunday covering safety, security, healthcare, on-chip learning and reactive programming.

The last two days of ESWEEK (Thursday and Friday) are dedicated to in-depth symposia and workshops covering topics like embedded multi-media, rapid system prototyping, approximate computing, industry-academia collaboration, CPS modeling, embedded OS, model-based development and embedded systems education.

Novel this year is the web page: It has undergone a new design and received additional content (for example an archive of previous ESWEEK events, a list of past best paper recipients etc.) and above all, it is now easy and convenient to browse from mobiles.

We want to thank all who made ESWEEK 2016 possible: The ESWEEK Organizing Committee, the ESWEEK Steering Committee, the Workshop and Symposia Organizers, MPA, the sponsors and all authors and speakers and attendees. Our special thanks go to Alex K. Jones the Local Arrangements Chair from the University of Pittsburg and his team for hosting ESWEEK 2016.

Have an inspiring, interesting and communicative ESWEEK 2016!



# GENERAL INFORMATION

## Welcome to Pittsburgh

ESWEEK 2016 will take place in Pittsburgh, Pennsylvania, USA.

Known colloquially as the “City of Bridges”, Pittsburgh is home to more bridges than even Venice! With world-class sports, nature, culture, and now the leading conference on Embedded Systems, you’re sure to find plenty to do in this great city.

Pittsburgh is a city in western Pennsylvania at the junction of 3 rivers. Its Gilded Age sites, including the Carnegie Museum of Natural History, the Carnegie Museum of Art and the Phipps Conservatory and Botanical Gardens, speak to its history as an early-20th-century industrial capital. In the North Shore neighborhood are the modern Andy Warhol Museum, Heinz Field football stadium and PNC Park baseball stadium.

## Conference Registration Fees

Conference registration allows attendance to any of the three ESWEEK conferences, CODES+ISSS, CASES, and EMSOFT. Conference registration includes lunch on conference days, online conference proceedings, the Sunday Welcome Reception, and one ticket to the banquet. Student Conference registration does not include a banquet ticket, but one can be purchased. Workshops, Tutorials, and Symposia can be added on to your registration for an additional fee.

Conference Member	<b>\$850</b>
Conference Non-Member	<b>\$975</b>
Conference Student Member	<b>\$500</b>
Conference Student Non-Member	<b>\$650</b>
Thursday Workshop	<b>\$300</b>
Thursday & Friday Workshops	<b>\$360</b>
Tutorial Only Full Day	<b>\$150</b>
Tutorial Only Half Day	<b>\$75</b>
Symposia Member	<b>\$375</b>
Symposia Non-Member	<b>\$440</b>





# ESWEEK 2016 OVERVIEW

## *Sunday, October 2*

Tutorials

Cocktail Reception

## *Monday, October 3*

Opening Session

Keynote by Srinu Devadas

CASES, CODES+ISSS, &  
EMSOFT Sessions

Poster Sessions

Technical Program  
Committee Dinner

## *Tuesday, October 4*

Keynote by Louis K. Scheffer

CASES, CODES+ISSS,  
EMSOFT & IoT Day Sessions

Poster Sessions

National Aviary - Social  
Event

## *Wednesday, October 5*

Keynote by Kaushik Roy

CASES, CODES+ISSS,  
EMSOFT & IoT Day  
Sessions

Poster Sessions

Best Paper Awards  
Ceremony

ESWEEK Panel

## *Thursday, October 6*

AC'16 Workshop

CAIRES'16 Workshop

CyPhy'16 Workshop

EWiLi'16 Workshop

HILT'16 Workshop

WESE'16 Workshop

RSP Symposium

ESTIMedia Symposium

## *Friday, October 7*

HILT'16 Workshop

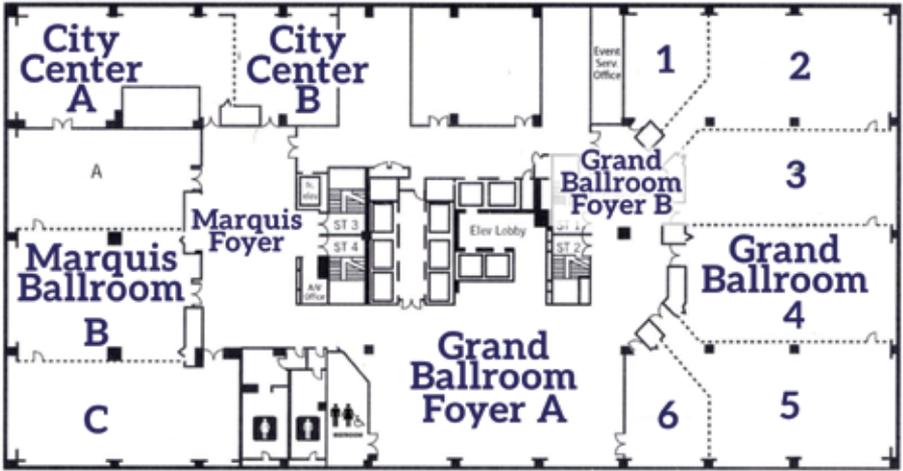
RSP Symposium

ESTIMedia Symposium



# CONFERENCE VENUE

## Conference Venue Floorplan



## Thank You to Our Platinum Sponsors



**HUAWEI**



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**SWANSON**  
ENGINEERING

COMPUTER ENGINEERING

**DeePhi** Tech focuses on deep learning, pushing the frontier of AI applications. Supported and invested by GSR Venture and Banyan Capital, we successfully developed a complete automation flow of compression, compiling and acceleration which achieves joint optimization between algorithm, software and hardware. A smaller, faster and more efficient deep learning processing unit (DPU) is released to public.

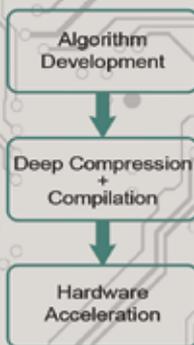


DeePhi has built deep collaboration with leading companies in fields of drone, security surveillance and cloud service. The FPGA based DPU platform achieves an order of magnitude higher energy efficiency over GPU on image recognition and speech detection. DeePhi believes a joint optimization between algorithm, software and hardware would be the trend of deep learning. Innovation and high quality research is our driving force to grow, quick iteration between products and customers makes us grow fast.

## Technologies

Algorithm, software, and hardware co-design, make deployment of deep learning algorithms simple, efficient and more accurate.

Team members of DeePhi Tech have worked on deep learning acceleration for years. Previous work were published at top machine learning and computer architecture conferences including NIPS, ICLR, FPGA, and ISCA. The technology of DeePhi is admitted by the industry and have been presented at Hot Chips 2016 together with Intel, ARM, Samsung, and other giants.



## Products

### Aristotle Architecture

Platform for CNN

Supports all networks

Supports object detection

### Descartes Architecture

Platform for RNN/LSTM

Supports speech recognition



DeePhi "Swift"  
DPU Platform





# BEST PAPER CANDIDATES

## CASES

### 3.2 LOCUS: LOW-POWER CUSTOMIZABLE MANY-CORE ARCHITECTURE FOR WEARABLES

**Authors:**

Cheng Tan - *National Univ. of Singapore*  
Adivi Kulkarni - *National Univ. of Singapore*  
Vanchinathan Venkataramani - *National Univ. of Singapore*  
Manupa Karunaratne - *National Univ. of Singapore*  
Tulika Mitra - *National Univ. of Singapore*  
Li-Shiuan Peh - *MIT*

### 3.3 D-PUF: AN INTRINSICALLY RECONFIGURABLE DRAM PUF FOR DEVICE AUTHENTICATION IN EMBEDDED SYSTEMS

**Authors:**

Soubhagya Sutar - *Purdue Univ.*  
Arnab Raha - *Purdue Univ.*  
Vijay Raghunathan - *Purdue Univ.*

### 4.2 CAFFEPRESSO: AN OPTIMIZED LIBRARY FOR DEEP LEARNING ON EMBEDDED ACCELERATOR-BASED PLATFORMS

**Authors:**

Gopalakrishna Hegde - *NTU Singapore*  
Siddhartha - *Nanyang Technological Univ.*  
Nachiappan Ramasamy - *NTU Singapore*  
Nachiket Kapre - *Nanyang Technological Univ.*

## CODES + ISSS

### 2.1 A DESIGN TO REDUCE WRITE AMPLIFICATION IN OBJECT-BASED NAND FLASH DEVICES

**Authors:**

Jie Guo - *Univ. of Pittsburgh*  
Chuhan Min - *Univ. of Pittsburgh*  
Tao Cai - *Jiangsu Univ.*  
Yiran Chen - *Univ. of Pittsburgh*

### 3.1 FAST AND CYCLE-ACCURATE SIMULATION OF MULTI-THREADED APPLICATIONS ON SMP ARCHITECTURES USING HYBRID PROTOTYPING

**Authors:**

Ehsan Saboori - *Concordia Univ.*  
Samar Abdi - *Concordia Univ.*

### 4.1 FAULT INJECTION AT HOST-COMPILED LEVEL WITH STATIC FAULT SET REDUCTION FOR SOC FIRMWARE ROBUSTNESS TESTING

**Authors:**

Petra R. Maier - *Technische Univ. München*  
Veit Kleeberger - *Infineon Technologies*  
Daniel Mueller-Gritschneider - *Technische Univ. München*  
Ulf Schlichtmann - *TU München*

## EMSOFT

### 3.1 LOCALLY OPTIMAL REACH SET OVER-APPROXIMATION FOR NONLINEAR SYSTEMS

**Authors:**

Chuchu Fan - *Univ. of Illinois at Urbana Champaign*  
James Kapinski - *Toyota Technical Center*  
Xiaoqing Jin - *Toyota Technical Center*  
Sayan Mitra - *Univ. of Illinois at Urbana Champaign*

### 3.2 UNDERMINER: A FRAMEWORK FOR AUTOMATICALLY IDENTIFYING NON-CONVERGENT BEHAVIORS IN BLACK BOX SYSTEM MODELS

**Authors:**

Ayca Balkan - *Univ. of California, Los Angeles*  
Paulo Tabuada - *Univ. of California, Los Angeles*  
Jyotirmoy Deshmukh - *Toyota Technical Center*  
Xiaoqing Jin - *Toyota Technical Center*  
James Kapinski - *Toyota Technical Center*

### 6.1 REAL-TIME CACHE MANAGEMENT FOR MULTI-CORE VIRTUALIZATION

**Authors:**

Hyoseung Kim - *Carnegie Mellon Univ.*  
Raj Rajkumar - *Carnegie Mellon Univ.*



# SUNDAY, OCTOBER 2 TUTORIALS SCHEDULE



## *Marquis A*

## *Marquis B*

## *Marquis C*

8:00 -  
12:00

AADL for Secure &  
Safe Systems Design &  
Analysis

IoT Security and  
Privacy Challenges  
and Solutions

When Embedded  
Systems meet Life  
Sciences: Microfluidic  
Biochips for Real-Time  
Healthcare

10:15 -  
10:30

Coffee Break | Room: Foyer

13:00 -  
14:00

Algorithms and  
Hardware for Learning  
On-a-Chip

IoT Security and  
Privacy Challenges  
and Solutions

Next-Generation  
Embedded Systems:  
Functional Reactive  
Programming, Formal  
Verification, and Real-  
Time Virtual Resources

14:00 -  
14:15

Coffee Break | Room: Foyer

14:15 -  
17:00

Algorithms and  
Hardware for Learning  
On-a-Chip

IoT Security and  
Privacy Challenges  
and Solutions

Next-Generation  
Embedded Systems:  
Functional Reactive  
Programming, Formal  
Verification, and Real-  
Time Virtual Resources

19:00 -  
22:00

Cocktail Reception | Room: City Center AB



## Tutorial 1 - AADL for Secure & Safe Systems Design & Analysis

**Time: 8:00 - 12:00 | Room: Marquis A**

This tutorial presents the Architecture Analysis & Design Language (AADL) for architecture modeling and demonstrates how to use the Open Source AADL Tool Environment (OSATE) to design and analyze architecture models and check their security and safety requirements. Attendees will design architecture models, annotate them with safety and security information, and use OSATE's built-in analysis tools to analyze system latency, safety, and security.

This interactive tutorial will encourage hands-on participation. Attendees can bring their laptops, use the OSATE modeling tool suite to follow the tutorial instructions, and learn how to design and analyze architecture models. We will provide instructions before the tutorial for installing the modeling tool so that attendees will be ready to use it.

### Biography:

Julien Delange is a senior member of the technical staff at the Carnegie Mellon Software Engineering Institute (SEI) in Pittsburgh, PA. He has been an active member of and contributor to the SAE AS-2C AADL standardization committee for more than 8 years. Julien has authored several research articles on architecture design and analysis, is a technical lead of the OSATE AADL modeling platform, and actively contributes to the Ocarina AADL code generator.

Before joining the SEI, Julien was a software engineer at the European Space Agency and worked on several research projects to design, analyze, and auto-produce safety-critical systems from models. He has a strong background in safety-critical systems and authored POK, the first open-source ARINC-653-compliant micro-kernel. He has a master's degree in computer science and embedded systems from University Pierre and Marie Curie in Paris and a doctorate in computer science from TELECOM-ParisTech in Paris, France.

### Speaker:

Julien Delange - *Carnegie Mellon Univ.*





## Tutorial 2 - When Embedded Systems meet Life Sciences: Microfluidic Biochips for Real-Time Healthcare

**Time: 8:00 - 12:00 | Room: Marquis C**

### Organizers:

Mirela Alistar - *Hasso-Plattner Institute*  
Krishnendu Chakrabarty - *Duke Univ.*  
Jan Madsen - *Technical Univ. of Denmark*  
Tsung-Yi Ho - *National Tsing Hua Univ.*  
Robert Wille - *Johannes Kepler Univ. of Linz*

This tutorial will provide the participants with first-hand experience on the emerging technology of digital microfluidic biochips. In addition to an introductory theory session, this tutorial offers a unique (and first-ever) hands-on lab, where the participants will directly interact with biochips.

First, the participants will be introduced to the envisioned use of biochips in synthetic biology and health care. Then, the participants will learn the technical challenges behind biochips, mainly the fluidic movement using electrowetting on dielectric and various fabrication techniques. Next, the tutorial will present an overview of the CAD tools for biochips focusing on their reliability in the presence of faults.

Afterwards, during a hands-on lab, the participants will experience all the steps of the workflow: application design, application synthesis, data collection and result interpretation. The participants will design their own application and execute it on an actual biochip. The hands-on lab will also provide a practical guide on custom fabrication of biochips.

### Biographies:

Mirela Alistar has been working since 2010 on developing tools for digital microfluidic biochips. As a complement to her academic track (publications, keynotes, etc), Mirela is supporting open access research and she has organized citizen-science events, where she disseminates to the public with the aim of involving them into creating more knowledge. She has been leading Biologigaragen (the biohacking space in Copenhagen) obtaining numerous governmental grants, and coaching the local universities on opening internal hackerspace. In 2016, she founded Bioflux, a startup with the vision of producing a widely used lab-on-a chip that can revolutionize healthcare and laboratory research.

Krishnendu Chakrabarty is the William H. Younger Distinguished Professor in the Department of Electrical and Computer Engineering at Duke University.

He is a recipient of many awards, including the Humboldt Research Award, the IEEE Trans. CAD Donald O. Pederson Best Paper award, 11 best paper awards at major conferences, and the IEEE Computer Society (CS) Technical Achievement Award. His current research is on design-for-testability of integrated circuits, microfluidic biochips, and cybermanufacturing. He is a Fellow of ACM, Fellow of IEEE, and Golden Core Member of the IEEE CS. Currently he serves as the Editor-in-Chief of IEEE Transactions on VLSI Systems.

Jan Madsen received his Ph.D. in Computer Science from Technical University of Denmark (DTU) in 1992. He is Full Professor in Computer-Based Systems at Department of Applied Mathematics and Computer Science at DTU. His research interests include design, modeling, analysis, optimization and construction of microelectronic, microfluidic and microbiological computing systems. He has published more than 150 peer-reviewed conference and journal papers. Since 2008 he has worked on Design Automation for microfluidic biochips, where he got a Best Paper Award at CASES 2009. Since 2011 he has coordinated research on synthetic biology with the vision to link it with biochip research.

Tsung-Yi Ho received his Ph.D. in Electrical Engineering from National Taiwan University in 2005. He is a Professor with the Department of Computer Science of National Tsing Hua University, Hsinchu, Taiwan. His research interests include design automation and test for microfluidic biochips and nanometer integrated circuits. He was a recipient of the Best Paper Awards at the VLSI Test Symposium (VTS) in 2013 and IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems in 2015.

Robert Wille received the Diploma and Dr.-Ing. degrees in computer science from the University of Bremen, Germany, in 2006 and 2009, respectively. Since 2015, he is full professor at the Johannes Kepler University Linz, Austria. His research interests include the development of design technologies for various application areas – with a particular focus on emerging technologies such as microfluidic biochips. This includes work in the domain of verification and proof engines as well as the synthesis and optimization. Since 2007, he published more than 130 journal and conference papers in this area and was repeatedly awarded.



## Tutorial 3 - Next-Generation Embedded Systems: Functional Reactive Programming, Formal Verification, and Real-Time Virtual Resources

*Time: 13:00 - 17:00 | Room: Marquis C*

Sophisticated digital systems are increasingly used to control complex physical components ranging from traditional stand-alone systems to highly-networked cyber-physical systems. Functional reactive programming (FRP) has several benefits over imperative programming for implementing embedded software, and can potentially transform the way we implement next-generation embedded systems. The first part of this tutorial introduces a framework for accurate response time analysis, scheduling, and verification of embedded controllers implemented as FRP programs.

Real-time resource partitioning divides hardware resources into temporal partitions and allocates these partitions as virtual resources to application tasks. Open embedded systems make it easy to add and remove software applications as well as to increase resource utilization and reduce implementation cost when compared to systems which physically assign distinct computing resources to run different applications. The second part of this tutorial describes ways to maintain the schedulability of real-time tasks as if they were scheduled on dedicated physical resources.

### Biography:

Albert M. K. Cheng is Professor and former interim Associate Chair of the Computer Science Department at the University of Houston. He received the B.A. with Highest Honors in Computer Science, graduating Phi Beta Kappa at age 19, the M.S. in Computer Science with a minor in Electrical Engineering at age 21, and the Ph.D. in Computer Science at age 25, all from The University of Texas at Austin, where he held a GTE Foundation Doctoral Fellowship. A recipient of numerous awards, Prof. Cheng has over 220 refereed publications and is author of the popular textbook entitled Real-Time Systems (Wiley).

### Speaker:

Albert M. K. Cheng - Univ. of Houston





## Tutorial 4 - Algorithms and Hardware for Learning On-a-Chip

**Time: 13:00 - 17:00 | Room: Marquis A**

Machine learning algorithms have made enormous progress in recent years. However their complexity still challenges the state-of-the-art computing platforms, especially when the application of interest is tightly constrained by the requirements of low power, high throughput and small latency. There is a timely research need to map the latest learning algorithms to application-specific systems, in order to achieve orders of magnitude improvement in performance, energy efficiency and compactness.

The overarching goal of this tutorial is to explore the potential of on-chip learning, to reveal algorithm and design needs, and to promote novel intelligent applications. The tutorial is organized to introduce the fundamental learning theories, discuss numerical algorithms and their complexity in implementation, explore representative hardware platforms and their performances, and present emerging applications in this field.

The intended audience of the tutorial include hardware designers, system architects and tool developers from various application domains who are interested in on-chip learning.

### Biographies:

Yu (Kevin) Cao received the Ph.D. degree in electrical engineering from University of California, Berkeley, in 2002. He is currently a Professor in the School of ECEE at Arizona State University. He has published numerous articles and two books on nano-CMOS modeling and physical design. His research interests include physical modeling of nanoscale technologies, design solutions for variability and reliability, reliable integration of post-silicon technologies, and hardware design for on-chip learning.

Xin Li received the Ph.D. degree in Electrical & Computer Engineering from Carnegie Mellon University in 2005. He is currently an Associate Professor in the ECE Department at Carnegie Mellon. His research interests include integrated circuit, signal processing and data analytics. Dr. Li was the Associate Editor of IEEE TBME, IEEE TCAD, ACM TODAES, IEEE D&T and JOLPE. He was the General Chair of ISVLSI and FAC. He received the NSF CAREER Award in 2012 and six Best Paper Awards from IEEE TCAD, DAC, ICCAD and ISIC.

### Speakers:

Yu (Kevin) Cao - *Arizona State Univ.*

Xin Li - *Carnegie Mellon Univ.*



## Tutorial 5 - IoT Security and Privacy Challenges and Solutions

*Time: 8:00 - 17:00 | Room: Marquis B*

Gartner estimates that a total of 26 billion connected devices will exist by the year 2020, with the majority being IoT and wearable devices. Security of these devices then becomes a great concern. In this tutorial, we give an overview of the challenges and tasks device manufacturers face when developing new devices and introducing themselves to a new market. We then cover some common pitfalls that we have encountered in our study of IoT and wearable devices. We provide detailed examples of our experimentation with devices with emphasis on the Nest Thermostat, the Nike+ Fuelband, the Centron Ultron C1SR electric meter, and other popular IoT devices. Lastly we conclude by presenting solutions that have been proposed by both industry and academia.

Besides the introduction to the IoT security problem, hands-on labs are also prepared for all audience. Modern and commercial IoT devices will be provided where audiences can practice how the devices can be compromised, causing device malfunction as well as other consequences.

### Biographies:

Yier Jin is an assistant professor of Computer Engineering at the University of Central Florida, an associate partner of the Intel Collective Research Institute for Secure Computing, and member of the Florida Institute of Cybersecurity. He holds a Ph.D. in Electrical Engineering from Yale University. His research has focused on developing methods for ensuring the security and trustworthiness of the integrated circuits and systems. He has contributed several key solutions in the areas of trusted hardware, IoT and CPS security, hardware IP/SoC Formal Verification, security enhanced processor architecture for cybersecurity, gate-level netlist reverse engineering, and emerging device design for hardware security.

Ahmad-Reza Sadeghi is a full professor of Computer Science at Technische Universität Darmstadt, Germany. He is the head of the System Security Lab at the Center for Advanced Security Research Darmstadt (CASED) and the Director of the Intel Collaborative Research Institute for Secure Computing (ICRI-SC) at TU-Darmstadt. He holds a Ph.D. in Computer Science from the University of Saarland in Saarbrücken, Germany. Prior to academia, he worked in Research and Development of Telecommunications enterprises, amongst others Ericsson Telecommunications.

Dean Sullivan\* and Orlando Arias\* (Hands-on Lab session student assistants)

### Speakers:

*Yier Jin - Univ. of Central Florida*

*Ahmad-Reza Sadeghi - Technische Univ. Darmstadt*



# MONDAY, OCTOBER 3 SCHEDULE OF EVENTS

Marquis A

Marquis B

Marquis C

8:15 (ct) -  
9:00

**ESWEEK Opening Session** | Room: Grand Ballroom

9:00 -  
10:00

**Monday Keynote:** *Srini Devadas, Massachusetts Institute of Technology,*  
"Secure Hardware Platforms for the Internet of Things (IoT)"  
Room: Grand Ballroom 1-3

10:00 -  
10:30

Coffee Break | Room: Foyer

10:30 -  
12:00

**CASES:** *Accelerators and High Level Synthesis*

**CODES+ISSS:** *Modeling and Simulation of Embedded Systems*

**EMSOFT:** *Timing and Energy-Aware Modeling and Programming of Embedded Systems*

12:00 -  
12:30

**Poster Session** | Room: Foyer

12:30 -  
14:00

Lunch | Room: Grand Ballroom 4-6  
F1/10 Autonomous Racing Demo | Room: Foyer

14:00 -  
15:30

**CASES:** *Reliability and Fault Tolerance*

**Special Session:**  
**CODES+ISSS:** *Time in Cyber-Physical Systems*

**EMSOFT:** *Providing QoS for Distributed Real-Time Systems*

15:30 -  
16:00

**Poster Session** | Room: Foyer

16:00 -  
17:30

**CASES:** *Application Driven Architectures: Security, Genetics and Wearables*

**CODES+ISSS:** *A Splash of Flash*

**EMSOFT:** *Verification and Synthesis of Embedded Control Systems*

17:30 -  
18:00

**Poster Session** | Room: Foyer  
F1/10 Autonomous Racing Tutorial | Room: Marquis Ballroom

19:30

**Technical Program Committee Dinner** | Carlton Restaurant

## Opening Session

*Time: 8:15(ct) - 9:00 | Room: Grand Ballroom*



### **Keynote: Secure Hardware Platforms for the Internet of Things (IoT)**

*Time: 9:00 - 10:00 | Room: Grand Ballroom 1-3*

#### **Keynote Speaker:**

*Srinivasa Devadas - Massachusetts Institute of Technology*

The Internet is expanding into the physical world, connecting billions of devices. In this Internet of Things, two contradictory trends are appearing. On the one hand, the cost of security breaches is increasing as we place more responsibilities on the devices that surround us. On the other hand, computing elements are becoming small, disseminated, unsupervised, and physically exposed. Unfortunately, existing computing systems do not address many new attacks, such as resource sharing and physical attacks, presenting a significant vulnerability in future embedded systems. Hardware to the rescue! This talk will describe how secure systems can be built from the ground up.

Physical Unclonable Functions (PUFs) are a tamper resistant way of establishing shared secrets with a physical device. They rely on the inevitable manufacturing variations between devices to produce private keys that can be used as a hardware root of trust in a secure processor. Architectural isolation can be used to secure computation on a remote secure processor with a private key where the privileged software is potentially malicious as recently shown by Intel's Software Guard Extensions (SGX). The Sanctum secure processor architecture offers the same promise as SGX, namely strong provable isolation of software modules running concurrently and sharing resources, but protects against an important class of additional software attacks that infer private information by exploiting resource sharing.

The Sanctum design and implementation is based on the RISC-V processor and is completely open source, allowing for independent analysis and formal

verification of security properties. The goal of the Sanctum project is to move secure hardware up to the level of scrutiny afforded by open source secure software.

#### **Biography:**

Srinivasa Devadas is the Webster Professor of Electrical Engineering and Computer Science at the Massachusetts Institute of Technology (MIT) where he has been on the faculty since 1988. He served as Associate Head of the Department of Electrical Engineering and Computer Science, with responsibility for Computer Science, from 2005 to 2011. Devadas's research interests span Computer-Aided Design (CAD), computer security and computer architecture and he has received significant awards from each discipline including the Richard Newton technical impact award and the IEEE Computer Society Technical Achievement award. He is a Fellow of the ACM and IEEE. He is a MacVicar Faculty Fellow and an Everett Moore Baker teaching award recipient, considered MIT's two highest undergraduate teaching honors.

#### **Chair:**

*Jörg Henkel - Karlsruhe Institute of Technology*



## CASES: Accelerators and High Level Synthesis

Time: 10:30 - 12:00 | Room: Marquis A

### Chair:

Aviral Shrivastava - *Arizona State Univ.*

#### 1.1 ILP-BASED MODULO SCHEDULING FOR HIGH-LEVEL SYNTHESIS

Julian Oppermann, Andreas Koch - *TU Darmstadt*

Melanie Reuter-Oppermann - *Karlsruhe Institute of Technology*

Oliver Sinnen - *Univ. of Auckland*

#### 1.2 ENABLING OPENVX SUPPORT IN MW-SCALE PARALLEL ACCELERATORS

Giuseppe Tagliavini - *Univ. of Bologna*

Germain Haugou - *ETH Zurich*

Andrea Marongiu - *Univ. of Bologna*

Luca Benini - *Università di Bologna*

#### 1.3 HANDLING LARGE DATA SETS FOR HIGH-PERFORMANCE EMBEDDED APPLICATIONS IN HETEROGENEOUS SYSTEMS-ON-CHIP

Paolo Mantovani, Emilio G. Cota, Christian Pilato, Giuseppe Di Guglielmo, Luca Carloni - *Columbia Univ.*

## CODES + ISSS: Modeling and Simulation of Embedded Systems

Time: 10:30 - 12:00 | Room: Marquis B

### Chair:

Daniel Müller-Gritschneider - *Technische Univ. München*

### Co-Chair:

Oliver Bringmann - *Tübingen Univ., Germany*

#### 1.1 A PRACTICAL METHODOLOGY TO VALIDATE THE STATISTICAL BEHAVIOR OF BLOOM FILTERS

Venkateshwar Kottapalli, Sunil Khatri - *Texas A&M Univ.*

#### 1.2 SCALABLE AND REALISTIC BENCHMARK SYNTHESIS FOR EFFICIENT NOC PERFORMANCE EVALUATION: A COMPLEX NETWORK ANALYSIS APPROACH

Yuankun Xue, Paul Bogdan - *Univ. of Southern California*

#### 1.3 AN ACCURATE AND FLEXIBLE EARLY MEMORY SYSTEM POWER EVALUATION APPROACH USING A MICROCOMPONENT METHOD

Chi-Kang Chen - *Industrial Technology Research Institute*

Hsin-I Wu, Chi-Ting Hsiao, Ren-Song Tsay - *National Tsing Hua Univ.*

## EMSOFT: Timing and Energy-Aware Modeling and Programming of Embedded Systems

Time: 10:30 - 12:00 | Room: Marquis C

### Chair:

Rolf Ernst - *Technische Univ. Braunschweig*

#### 1.1 INVITED EMBEDDED TUTORIAL: ENERGY CONSUMPTION IN EMBEDDED SYSTEMS: ABSTRACTIONS FOR SOFTWARE MODELS, PROGRAMMING LANGUAGES, AND VERIFICATION METHODS

Florence Maraninchi - *Verimag*

#### 1.2 ENERGY AND TIMING AWARE SYNCHRONOUS PROGRAMMING

JiaJie Wang, Partha S. Roop - *Univ. of Auckland*  
Alain Girault - *INRIA Grenoble - Rhône-Alpes*

#### 1.3 FLEXIBLE SUPPORT FOR TIME AND COSTS IN SCENARIO-AWARE DATAFLOW

Michael Bungert - *Saarland Univ.*  
Arnd Hartmanns - *Univ. of Twente*  
Holger Hermanns - *Saarland Univ.*

## F1/10 Autonomous Racing Demo at ESWeek

*Time: 12:30 | Room: Foyer*

The F1/10 competition focuses on creating a meaningful and challenging design experience for students. The competition involves designing, building, and testing an autonomous 1/10th scale F1 race car (capable of speeds in excess of 40MPH) all while learning about perception, planning, and control for autonomous navigation.

F1/10 team is creating the infrastructure necessary to allow anybody to build, drive, and race their own autonomous race car. From teams new to controls engineering, to seasoned controller designers, the content available on F1Tenth.org is engaging and informative for all audiences. Together, we are making autonomy accessible and exciting.

## CASES: Reliability and Fault Tolerance

*Time: 14:00 - 15:30 | Room: Marquis A*

### Chair:

Jingtong Hu - *Oklahoma State Univ.*

### 2.1 RUNTIME MANAGEMENT OF ADAPTIVE MPSOCS FOR GRACEFUL DEGRADATION

Stavros Tzilis, Ioannis Sourdis - *Chalmers Univ. of Technology*

Vasileios Vasilikos - *Kenotom P.C. - I.K.E.*

Dimitrios Rodopoulos - *IMEC*

Dimitrios Soudris - *National Technical Univ. of Athens*

### 2.2 TOWARDS THE DESIGN OF FAULT-TOLERANT MIXED-CRITICALITY SYSTEMS ON MULTICORES

Luyuan Zeng, Pengcheng Huang - *ETH Zurich*

Lothar Thiele - *Swiss Federal Institute of Technology Zurich*

### 2.3 COMET: COMMUNICATION-OPTIMISED MULTI-THREADED ERROR-DETECTION TECHNIQUE

Konstantina Mitropoulou,  
Vasileios Porpodas, Timothy M. Jones  
- *Univ. of Cambridge*





## Special Session: CODES + ISSS: Time in Cyber-Physical Systems

*Time: 14:00 - 15:30 | Room: Marquis B*

### Organizer:

*Aviral Shrivastava - Arizona State Univ.*

Cyber-Physical systems are those that tightly integrate physical and computational systems. One of the big challenges in distributed cyber-physical systems is establishing a common notion of time between the physical world and the computational system. Many modern CPS, especially industrial automation systems, require the actions of different computational systems to be synchronized at much higher rates than is possible through adhoc designs. Fundamental research is needed in synchronizing clocks of computing systems to a higher degree, and even if the clocks are synchronized, designing CPS nodes so that they can perform actions in a synchronized manner is challenging. We need to find ways to specify distributed CPS applications, ways to specify and verify timing requirements on distributed CPS, confident top-down design methodologies that can ensure the system meets its timing requirements in the first go, dynamically creating and dissolving timing domains using differently build components, and much more.

Cyber Physical Systems are the next generation of more complex embedded systems. CPS are multidisciplinary in the sense that designing CPS requires the knowledge of mechanical, electrical, embedded systems, and control theory. While CODES+ISSS recognizes the importance of this challenge-domain, and welcomes and includes research papers in this direction, a top-down, vertical perspective of this active and important area of inquiry is often absent in the paper presentations.

This special session comprises of speakers from industry, academia and government agencies, all coming in to give an overview of time-related challenges facing the industry and society. We will also go over the state-of-the-art and its limitations, what problems are somewhat solved, and where much more research is needed. Finally, we will present an overview of the CPS testbed that has been developed to test the timing of distributed CPS, and evaluate the effectiveness of timing-correct-by-construction methodologies.

### 1SS.1 TIMING IN CPS

*Ya-Shian Li-Baboud - National Institute of Standards and Technology*

### 1SS.2 TIME AND TIMELINESS

*Kevin Stanton - Intel Corp.*

### 1SS.3 PROGRAMMING WITH TIME

*Patricia Derler - National Instruments Corp.*

### 1SS.4 TIMING TESTBED

*Aviral Shrivastava - Arizona State Univ.*

## EMSOFT: Providing QoS for Distributed Real-Time Systems

*Time: 14:00 - 15:30 | Room: Marquis C*

### Chair:

*Paul Bogdan - Univ. of Southern California*

### 2.1 INVITED EMBEDDED TUTORIAL: LESSONS LEARNED ON ASSUMPTIONS AND SCALABILITY WITH TIME-AWARE INSTRUMENTATION

*Sebastian Fischmeister, Guy Martin  
Tchamgoue - Univ. of Waterloo*

### 2.2 MAKING DDS REALLY REAL-TIME WITH OPENFLOW

*Hyon-Young Choi, Andrew King, Insup Lee -  
Univ. of Pennsylvania*

### 2.3 EXPLORING THE PERFORMANCE OF ROS2

*Yuya Maruyama - Osaka Univ.  
Shinpei Kato - The Univ. of Tokyo  
Takuya Azumi - Osaka Univ.*



## CASES: Application Driven Architectures: Security, Genetics and Wearables

**Time: 16:00 - 17:30 | Room: Marquis A**

### Chair:

Oliver Bringmann - *Univ. Tübingen*

### 3.1 A REAL-TIME DIGITAL-MICROFLUIDIC PLATFORM FOR EPIGENETICS

Mohamed Ibrahim, Craig Boswell, Krishnendu Chakrabarty, Kristin Scott, Miroslav Pajic - *Duke Univ.*

### 3.2 \* LOCUS: LOW-POWER CUSTOMIZABLE MANY-CORE ARCHITECTURE FOR WEARABLES

Cheng Tan, Aditi Kulkarni, Vanchinathan Venkataramani, Manupa Karunaratne, Tulika Mitra - *National Univ. of Singapore*  
Li-Shiuan Peh - *MIT*

- 3.3 \* D-PUF: AN INTRINSICALLY RECONFIGURABLE DRAM PUF FOR DEVICE AUTHENTICATION IN EMBEDDED SYSTEMS  
Soubhagya Sutar, Arnab Raha, Vijay Raghunathan - *Purdue Univ.*

## CODES + ISSS: A Splash of Flash

**Time: 16:00 - 17:30 | Room: Marquis B**

### Chair:

Lars Bauer - *Karlsruhe Institute of Technology*

### Co-Chair:

Aviral Shrivastava - *Arizona State Univ.*

### 2.1 \* A DESIGN TO REDUCE WRITE AMPLIFICATION IN OBJECT-BASED NAND FLASH DEVICES

Jie Guo, Chuhan Min - *Univ. of Pittsburgh*  
Tao Cai - *Jiangsu Univ.*  
Yiran Chen - *Univ. of Pittsburgh*

- 2.2 HOW TO ENABLE SOFTWARE ISOLATION AND BOOST SYSTEM PERFORMANCE WITH SUB-BLOCK ERASE OVER 3D FLASH MEMORY  
Hsin-Yu Chang, Chien-Chung Ho - *National Taiwan Univ.*  
Yuan-Hao Chang - *Academia Sinica*  
Yu-Ming Chang - *Macronix International Co. Ltd.*  
Tei-Wei Kuo - *Academia Sinica & National Taiwan Univ.*

### 2.3 REALIZING ERASE-FREE SLC FLASH MEMORY WITH REWRITABLE PROGRAMMING DESIGN

Yu-Ming Chang, Yung-Chun Li, Ping-Hsien Lin, Hsiang-Pang Li - *Macronix International Co. Ltd.*  
Yuan-Hao Chang - *Academia Sinica*

**EMSOFT: Verification and Synthesis of Embedded Control Systems***Time: 16:00 - 17:30 | Room: Marquis C***Chair:***Oleg Sokolsky - Univ. of Pennsylvania***3.1 \*LOCALLY OPTIMAL REACH SET OVER-APPROXIMATION FOR NONLINEAR SYSTEMS***Chuchu Fan - Univ. of Illinois at Urbana Champaign**James Kapinski - Toyota Technical Center**Xiaoqing Jin - Toyota Technical Center**Sayan Mitra - Univ. of Illinois at Urbana**Champaign***3.2 \*UNDERMINER: A FRAMEWORK FOR AUTOMATICALLY IDENTIFYING NON-CONVERGENT BEHAVIORS IN BLACK BOX SYSTEM MODELS***Ayca Balkan, Paulo Tabuada - Univ. of California, Los Angeles**Jyotirmoy Deshmukh - Toyota Technical Center**Xiaoqing Jin - Toyota Technical Center**James Kapinski - Toyota Technical Center***3.3 ROBUST CONTROLLER SYNTHESIS OF SWITCHED SYSTEMS USING COUNTEREXAMPLE GUIDED FRAMEWORK***Hadi Ravanbakhsh, Sriram Sankaranarayanan - Univ. of Colorado***Tutorial: F1/10 Autonomous Racing***Time: 17:30 | Room: Marquis Ballroom***\*\*\*\*\* NO REGISTRATION FEES REQUIRED! \*\*\*\*\***

It is often said in racing that 'if everything seems under control then you're not going fast enough'.

In the F1/10 autonomous racing competition, teams use the same 1/10th scale platform to race against each other and test limits of their control.

The cars can reach racing speeds of up to 40mph !

In this tutorial you will learn about the principles of real-time perception, planning, and control for autonomous navigation. We will cover the hardware and software necessary to BUILD, DRIVE, and RACE a 1/10th scale F1 autonomous race car.

This is a very practical tutorial: all instruction is directly relevant to building and running the race car we have developed. The goal is to enable students and researchers with various backgrounds to start their own autonomous racing effort and jump-start an autonomous race competition!

More info at <http://f1tenth.org/>

**Organizers:**

Madhur Behl and Rahul Mangharam

University of Pennsylvania



# TUESDAY, OCTOBER 4 SCHEDULE OF EVENTS

Marquis A

Marquis B

Marquis C

City Center AB

8:15 -  
9:00

Breakfast | Room: Foyer

9:00 -  
10:00

Tuesday Keynote: Louis K. Scheffer, Howard Hughes Medical Institute  
"Learning from Life" | Room: Grand Ballroom 1-3

10:00 -  
10:30

Coffee Break | Room: Foyer

10:30 -  
12:00

**CASES:**  
*Architectures for  
Machine Learning*

**CODES+ISSS:**  
*System-Level  
Design*

**EMSOFT:**  
*Verification of  
Hybrid Systems*

**IoT Day:** *Internet  
of Things:  
Technologies  
and Application  
Challenges*

12:00 -  
12:30

Poster Session | Room: Foyer

12:30 -  
14:00

Lunch | Room: Grand Ballroom 4-6

14:00 -  
15:30

**Special Session:**  
**CASES:**  
*Power and  
Thermal  
Management  
in Massive  
Multicore Chips:  
Theoretical  
Foundation meets  
Architectural  
Innovation  
and Resource  
Allocation*

**Special Session:**  
**CODES+ISSS:**  
*Harnessing the  
Power of Big  
Data - Computing  
Technology to  
Transform Big  
Data into Insight*

**EMSOFT:**  
*Efficient and  
Adaptive Resource  
Management  
and Hardware  
Abstraction*

**IoT Day:** *Self-aware  
Systems for the  
Internet-of-Things*

15:30 -  
16:00

Poster Session | Room: Foyer

16:00 -  
17:30

**CASES:** *Binary  
Code Analysis  
and Debugging*

**CODES+ISSS:**  
*Reliability and  
Robustness*

**EMSOFT:**  
*Timing Analysis  
and Cache  
Management with  
Multi-Level Caches  
in Real-Time  
Systems*

**IoT Day:** *Making the  
Internet-of-Things a  
Reality: From Smart  
Models, Sensing  
and Actuation to  
Energy-Efficient  
Architectures 4*

17:30 -  
18:00

Poster Session | Room: Foyer

18:30 -  
22:00

National Aviary - Social Event



## Keynote: Learning from Life

**Time: 9:00 - 10:00 | Room: Grand Ballroom 1-3**

### Keynote Speaker:

Louis K. Scheffer - *Howard Hughes Medical Institute*

Despite a half century of concerted effort, our best hardware and software combined still struggles to perform tasks that living organisms do effortlessly. Examples include object recognition, generalizing from few examples, and orchestrating collective behavior. For these and similar problems, decades of applying more and more computer power have realized only limited gains, making it clear the root problem is our lack of understanding of how to approach these tasks. One obvious path to cracking these problems is to understand how the brain solves them, but until now, this has always been at least as difficult as improving existing algorithms.

However, modern tools are finally becoming equal to the task of researching the brain, while progress on improving existing techniques remains incremental. So perhaps the most productive approach towards significant improvements in our hardware and software is to understand how the brain works, then copy these capabilities into man-made systems. Along these lines, we look at a few examples of how software and hardware might evolve, based upon what we already know of the brain.

### Biography:

Lou Scheffer was trained as a EE at Caltech and Stanford. He spent the next 30 years designing both integrated circuits, and the software tools used to design them, at Hewlett Packard and Cadence. In 2008, he switched fields, moving to studying the brain at the Howard Hughes Medical Institute. There his research interests include methods to derive the detailed structure of the brain, and using this information to try to figure out how it works. His outside interests include SETI (the search for extraterrestrial life), and science education. He is the author of the usual collection of papers, books, and patents.

### Chair:

Lothar Thiele - *ETH Zurich*

## CASES: Architectures for Machine Learning

**Time: 10:30 - 12:00 | Room: Marquis A**

### Chair:

Jörg Henkel - *Karlsruhe Institute of Technology*

#### 4.1 HYBRID NETWORK-ON-CHIP ARCHITECTURES FOR ACCELERATING DEEP LEARNING KERNELS ON HETEROGENEOUS MANYCORE PLATFORMS

Wonje Choi, Karthi Duraisamy - *Washington State Univ.*

Ryan Kim - *Carnegie Mellon Univ.*

Janardhan Rao Doppa, Partha Pande - *Washington State Univ.*

Radu Marculescu, Diana Marculescu - *Carnegie Mellon Univ.*

#### 4.2 \* CAFFEPRESSO: AN OPTIMIZED LIBRARY FOR DEEP LEARNING ON EMBEDDED ACCELERATOR-BASED PLATFORMS

Gopalakrishna Hegde - *NTU Singapore*

Siddhartha - *Nanyang Technological Univ.*

Nachiappan Ramasamy - *NTU Singapore*

Nachiket Kapre - *Nanyang Technological Univ.*

#### 4.3 MATRIX MULTIPLICATION BEYOND AUTO-TUNING: REWRITE-BASED GPU CODE GENERATION

Michel Steuwer, Toomas Rimmelg,

Christophe Dubach - *The Univ. of Edinburgh*



## IOT Day: Internet of Things: Technologies and Application Challenges

Time: 10:30 - 12:00 | Room: City Center AB

### Chair:

Arif Merchant - *Google Inc.*

### 2SS.1 IOT TECHNOLOGIES FOR EMBEDDED COMPUTING: A SURVEY

Farzad Samie, Lars Bauer, Jörg Henkel - *Karlsruhe Institute of Technology*

### 2SS.2 DISTRIBUTED QOS MANAGEMENT FOR INTERNET OF THINGS UNDER RESOURCE CONSTRAINTS

Farzad Samie - *Karlsruhe Institute of Technology*  
Vasileios Tsoutsouras, Sotirios Xydis - *National Technical Univ. of Athens*,  
Lars Bauer - *Karlsruhe Institute of Technology*,  
Dimitrios Soudris - *National Technical Univ. of Athens*  
Jörg Henkel - *Karlsruhe Institute of Technology*

### 2SS.3 EVOLVING AUTHENTICATION DESIGN CONSIDERATIONS FOR THE INTERNET OF BIOMETRIC THINGS (IOBT)

Nima Karimianbahnemiri, Paul Wortman, Fatemen Tehranipoor - *Univ. of Connecticut*

## CODES + ISSS: System-Level Design

Time: 10:30 - 12:00 | Room: Marquis B

### Chair:

Hyunok Oh - *Hanyang Univ.*

### Co-Chair:

Paul Bogdan - *Univ. of Southern California*

### 3.1 \*FAST AND CYCLE-ACCURATE SIMULATION OF MULTI-THREADED APPLICATIONS ON SMP ARCHITECTURES USING HYBRID PROTOTYPING

Ehsan Saboori, Samar Abdi - *Concordia Univ.*

### 3.2 EFFICIENT DESIGN SPACE EXPLORATION BY KNOWLEDGE TRANSFER

Dandan Li, Senzhang Wang, Shuzhen Yao - *Beihang Univ.*  
Yu-Hang Liu - *Chinese Academy of Sciences*  
Yuanqi Cheng - *Beihang Univ.*  
Xian-He Sun - *Illinois Institute of Technology*

### 3.3 OPTIMAL FUNCTIONAL-UNIT ASSIGNMENT AND BUFFER PLACEMENT FOR PROBABILISTIC PIPELINES

Weiwen Jiang, Edwin Sha, Qingfeng Zhuge, Xianzhang Chen - *Chongqing Univ.*



## EMSOFT: Verification of Hybrid Systems

**Time: 10:30 - 12:00 | Room: Marquis C**

### Chair:

Miroslav Pajic - *Duke Univ.*

#### 4.1 AN ALGORITHMIC APPROACH TO GLOBAL ASYMPTOTIC STABILITY VERIFICATION OF HYBRID SYSTEMS

Miriam García Soto - *IMDEA Software Institute*,  
Pavithra Prabhakar - *Kansas State Univ.*

#### 4.2 VERIFYING CYBER-PHYSICAL SYSTEMS BY COMBINING SOFTWARE MODEL CHECKING WITH HYBRID SYSTEMS REACHABILITY

Stanley Bak - *United States Air Force Research Lab*  
Sagar Chaki - *Carnegie Mellon Univ.*

#### 4.3 DARBOUX-TYPE BARRIER CERTIFICATES FOR SAFETY VERIFICATION OF NONLINEAR HYBRID SYSTEMS

Xia Zeng - *East China Normal Univ.*  
Wang Lin - *Wenzhou Univ.*  
Zhengfeng Yang - *East China Normal Univ.*  
Xin Chen - *Nanjing Univ.*  
Lilei Wang - *East China Normal Univ.*

## Special Session: CASES: Power and Thermal Management in Massive Multicore Chips: Theoretical Foundation meets Architectural Innovation and Resource Allocation

**Time: 14:00 - 15:30 | Room: Marquis A**

### Organizer:

Paul Bogdan - *Univ. of Southern California*

The realization of the promise of massive-scale integration depends on solutions to the problems of escalating power consumption and subsequent reduced reliability. Continuing progress and integration levels in silicon technologies make possible complete end-user systems consisting of extremely high number of cores on a single chip targeting either embedded or high-performance computing. However, without new paradigms of energy- and thermally-efficient designs, producing information and communication systems capable of meeting the computing, storage and communication demands of the emerging applications will be unlikely. The broad topic of power and thermal management of massive multicore chips is actively being pursued by a number of researchers worldwide, from a variety of different perspectives, ranging from workload modeling to efficient on-chip network infrastructure to resource allocation.

Successful solutions will likely adopt and encompass elements from all or at least several levels of abstraction. In this special session, we will present the Power-Thermal-Performance (PTP) trade-offs of massive multicore processors by considering three inter-related but varying angles, viz. on-chip traffic modeling, novel Networks-on-Chip (NoC) architecture and resource allocation.

#### 1SS.1 THEORETICAL FOUNDATIONS FOR WORKLOAD MODELING WITH IMPLICATIONS ON POWER OPTIMIZATION

Paul Bogdan - *Univ. of Southern California*

#### 1SS.2 PERFORMANCE AND POWER MANAGEMENT IN WIRELESS NOC-ENABLED MULTICORE CHIPS

Partha Pande - *Washington State Univ.*

#### 1SS.3 THERMAL-DRIVEN RESOURCE ALLOCATION AND APPLICATION MAPPING FOR COMPLEX MANY CORE SYSTEMS

Jörg Henkel - *Karlsruhe Institute of Technology*



## Special Session: CODES + ISSS: Harnessing the Power of Big Data - Computing Technology to Transform Big Data into Insight

Time: 14:00 - 16:00 | Room: Marquis B

### Organizers:

Houman Homayoun - *George Mason Univ.*  
Farinaz Koushanfar - *Univ. of California at San Diego*

Extracting useful knowledge from the massive volume of data generated by various sources is introducing a paradigm shift in the way people and organizations proceed and interact with each other. While several advances in branches of technology – data sensing, communication, computation, and storage promise enabling the new applications, the computational complexity and variety of big data applications challenges the state-of-the-art algorithms and computing platforms. General-purpose one-size fits all solutions are unlikely to handle the vast spectrum of applications and computing domain options. This special session explores the potential of automated optimization and mapping of machine learning algorithms and their design needs. We will discuss the real-world challenges and opportunities faced for performing novel massive data analytics while considering various constraints. Particular focus will be on end-to-end specialized solutions that tune the application and data analysis algorithms to the underlying architecture with the objective of meeting the performance and cost constraints.

### 2SS.1 AN OVERVIEW OF MICRON'S AUTOMATA PROCESSOR

Ke Wang, Kevin Angstadt, Chunkun Bo, Nathan Brunelle, Elaheh Sadredini, Tommy Tracy II, Jack Wadden, Mircea Stan, Kevin Skadron - *Univ. of Virginia*

### 2SS.2 ENABLING THE HIGH LEVEL SYNTHESIS OF DATA ANALYTICS ACCELERATORS

Marco Minutoli - *Pacific Northwest National Lab*  
Vito Giovanni Castellana - *Polytechnic Univ. of Milan*  
Antonino Tumeo - *Pacific Northwest National Lab*  
Marco Lattuada, Fabrizio Ferrandi - *Politecnico di Milano*

### 2SS.3 BIG DATA ANALYTICS ON HETEROGENEOUS ACCELERATOR ARCHITECTURES

Avesta Sasan - *Broadcom Corp.*  
Houman Homayoun, Katayoun Neshatpour - *George Mason Univ.*

### 2SS.4 GOING DEEPER THAN DEEP LEARNING FOR MASSIVE DATA ANALYTICS UNDER PHYSICAL CONSTRAINTS

Bitra D. Rouhani - *Univ. of California at San Diego*  
Azalia Mirhoseini - *Google, Inc.*  
Farinaz Koushanfar - *Univ. of California at San Diego*

## Special Session: IoT Day: Self-aware Systems for the Internet-of-Things

Time: 14:00 - 15:30 | Room: City Center AB

### Organizer:

Rolf Ernst - *Technische Univ. Braunschweig*  
The IoT will host a large number of co-existing cyber-physical applications. Continuous change, application interference, environment dynamics and uncertainty lead to complex effects which must be controlled to give performance and application guarantees. Application and platform self-configuration and self-awareness are one paradigm to approach this challenge. They can leverage context knowledge to control platform and application functions and their interaction. They could play a dominant role in large scale cyber-physical systems and systems-of-systems, simply because no person can oversee the whole system functionality and dynamics. IoT adds a new dimension because Internet based services will increasingly be used in such system functions. Autonomous vehicles accessing cloud services for efficiency and comfort as well as to reach the required level of safety and security are an example. Such vehicle platforms will communicate with a service infrastructure that must be reliable and highly responsive.

Automated continuous self-configuration of data storage might be a good basis for such services up to the point where the different self-x strategies might affect each other, in a positive or negative form. The session will have 3 talks, "Self-aware Computing and the Internet of (Adaptive) Things" by Henry Hoffmann, University of Chicago, "Controlling Concurrent Change - A self-aware infrastructure for continuous change and evolution in automotive systems" by Rolf Ernst, TU Braunschweig, and "A big data approach to optimizing storage" by Arif Merchant, Google Research.

### 3SS.1 SELF-AWARE COMPUTING AND THE INTERNET OF (ADAPTIVE) THINGS

Henry Hoffmann - *Univ. of Chicago*

### 3SS.2 CONTROLLING CONCURRENT CHANGE - A SELF-AWARE INFRASTRUCTURE FOR CONTINUOUS CHANGE AND EVOLUTION IN AUTOMOTIVE SYSTEMS

Rolf Ernst - *Technische Univ. Braunschweig*

### 3SS.3 A BIG DATA APPROACH TO OPTIMIZING STORAGE

Arif Merchant - *Google, Inc.*



## EMSOFT: Efficient and Adaptive Resource Management and Hardware Abstraction

**Time: 14:00 - 15:30 | Room: Marquis C**

### Chair:

Alain Girault - *Inria Grenoble - Rhône-Alpes*

### 5.1 A FLATTENED HIERARCHICAL SCHEDULER FOR REAL-TIME VIRTUALIZATION

Michael Drescher, Vincent Legout, Antonio Barbalace, Binoy Ravindran - *Virginia Tech*

### 5.2 RMC: AN INTEGRATED RUNTIME SYSTEM FOR ADAPTIVE MANY-CORE COMPUTING

Jinsu Park, Eunbi Cho, Woongki Baek - *UNIST*

### 5.3 AUTOMATIC HAL GENERATION FOR EMBEDDED MULTIPROCESSOR SYSTEMS

Merten Popp, Orlando Moreira, Wim Yedema, Menno Lindwer - *Intel Corp.*

## CASES: Binary Code Analysis and Debugging

**Time: 16:00 - 17:30 | Room: Marquis A**

### Chair:

Henri-Pierre Charles - *CEA-LIST*

### 5.1 SPECULATIVE DISASSEMBLY OF BINARY CODE

M. Ammar Ben Khadra, Dominik Stoffel, Wolfgang Kunz - *Univ. of Kaiserslautern*

### 5.2 A JUMP-TARGET IDENTIFICATION METHOD FOR MULTI-ARCHITECTURE STATIC BINARY TRANSLATION

Alessandro Di Federico, Giovanni Agosta - *Politecnico di Milano*

### 5.3 ON-THE-FLY LOAD DATA VALUE TRACING IN MULTICORES

Mounika Ponugoti, Amrish Tewar, Aleksandar Milenkovic - *The Univ. of Alabama in Huntsville*

## Special Session: IoT Day: Making the Internet-of-Things a Reality: From Smart Models, Sensing and Actuation to Energy-Efficient Architectures

**Time: 16:00 - 17:30 | Room: City Center AB**

### Organizer:

Paul Bogdan - *Univ. of Southern California*

Advances in the physical sciences and engineering enable the development of internet-of-things (IoT) to understand, interface / interact and engineer physical world (systems). However, the deployment of multitude of wireless sensors and agents spanning many application domains (e.g. environmental, healthcare, smart interconnected automobiles and trucks, smart buildings) leads not only to tremendous requirements for communicating massive amounts of multiscale heterogeneous data, but also raises a number of outstanding challenges: (1) How can we construct efficient machine learning algorithms to construct mathematical models of the sensed data to enable better analysis, prediction and control? (2) How to overcome the energy wall in the IoT architecture while considering the computation, communication and control perspectives in a unified way? (3) How to design a decentralized control while ensuring composability in the IoT?

(4) How can the closed-loop control be enforced and brought closer to the sensing location to avoid the data movement and communication costs? To address these outstanding challenges, out-of-the-box approaches need to be explored.

### 4SS.1 COMPACT YET ACCURATE MATHEMATICAL MODELING OF COMPLEX SYSTEMS

Paul Bogdan - *Univ. of Southern California*

### 4SS.2 DESIGN CONSIDERATIONS FOR ARCHITECTING ULTRA-LOW POWER IOT EDGE DEVICES

Vijay Raghunathan - *Purdue Univ.*

### 4SS.3 CLOSING THE LOOP: COMPOSABLE ARCHITECTURES FOR REAL-TIME CONTROL OVER WIRELESS NETWORKS

Miroslav Pajic - *Duke Univ.*

### 4SS.4 ENERGY-EFFICIENT MANYCORE ARCHITECTURES FOR IOT APPLICATIONS

Partha Pratim Pande - *Washington State Univ.*

## CODES + ISSS: Reliability and Robustness

Time: 16:00 - 17:30 | Room: Marquis B

### Chair:

Roman Lysecky - *Univ. of Arizona*

### Co-Chair:

Yier Jin - *Univ. of Central Florida*

#### 4.1 \*FAULT INJECTION AT HOST-COMPILED LEVEL WITH STATIC FAULT SET REDUCTION FOR SOC FIRMWARE ROBUSTNESS TESTING

Petra R. Maier - *Technische Univ. München*

Veit Kleeberger - *Infineon Technologies*

Daniel Mueller-Gritschneider - *Technische Univ. München*

Ulf Schlichtmann - *TU München*

#### 4.2 OPTIMIZING THE LOCATION OF ECC PROTECTION IN NETWORK-ON-CHIP

Junshi Wang - *Univ. of Electronic Science and Technology of China*

Letian Huang - *Univeristy of Electronic Science and Technology of China*

Qiang Li, Guangjun Li - *Univ. of Electronic Science and Technology of China*

Axel Jantsch - *TU Wien*

#### 4.3 A DISTURBANCE-AWARE SUB-BLOCK DESIGN TO IMPROVE RELIABILITY OF 3D MLC FLASH MEMORY

Hung-Sheng Chang - *National Taiwan Univ.*

Yuan-Hao Chang - *Academia Sinica*

Tei-Wei Kuo - *Academia Sinica & National Taiwan Univ.*

Yu-Ming Chang, Hsiang-Pang Li - *Macronix International Co. Ltd.*

## EMSOFT: Timing Analysis and Cache Management with Multi-Level Caches in Real-Time Systems

Time: 16:00 - 17:30 | Room: Marquis C

### Chair:

Marco Bekooij - *Univ. of Twente + NXP Semiconductors*

#### 6.1 \*REAL-TIME CACHE MANAGEMENT FOR MULTI-CORE VIRTUALIZATION

Hyoseung Kim, Raj Rajkumar - *Carnegie Mellon Univ.*

#### 6.2 CACHE-RELATED PREEMPTION DELAY ANALYSIS FOR MULTI-LEVEL INCLUSIVE CACHES

Zhenkai Zhang, Xenofon Koutsoukos - *Vanderbilt Univ.*



# WEDNESDAY, OCTOBER 5 SCHEDULE OF EVENTS

Marquis A

Marquis B

Marquis C

City Center AB

8:15 -  
9:00

Breakfast Room: Foyer

9:00 -  
10:00

Wednesday Keynote: Kaushik Roy, Purdue Univ. "Approximate Computing for Energy-efficient Error-resilient Systems" | Room: Grand Ballroom 1-3

10:00 -  
10:30

Coffee Break

10:30 -  
12:00

**CASES:** Memory Management

**CODES+ISSS:**  
Hungry for Power: Energy Efficiency in Heterogeneous Multiprocessors

**EMSOFT:**  
Autonomous Systems and their Verification

**IoT Day:** Internet-of-Things: Key Enablers and Assistive Technologies

12:00 -  
12:30

Poster Session | Room: Foyer

12:30 -  
14:00

Lunch | Room: Grand Ballroom 4-6

14:00 -  
15:30

**Special Session:**  
**CASES:**  
Eastern Wisdom: Neuromorphic Computing Research in China

**Special Session:**  
**CODES+ISSS:**  
I am a Chip, Therefore: Can I Think? - The Dawn of Self-Awareness in Cyber-Physical Systems

**EMSOFT:** Formal Methods for Robust and Predictable Embedded Systems

**EMSOFT:** Techniques for Real-Time Task and Communication Scheduling

15:30 -  
16:00

Poster Session Room: Foyer

16:00 -  
17:30

**CODES+ISSS:**  
Energy-Aware Embedded System Architectures

**CODES+ISSS:**  
Acceleration of Analytic Workloads

**EMSOFT:**  
Management of Flash-Based and Hybrid Memory Systems for Improved Latency, Lifetime, and Reliability

17:30 -  
18:00

Poster Session | Room: Foyer

18:00 -  
19:30

Best Paper Awards Ceremony & ESWEEK Panel: Embedded Systems Challenges in the Era of Cyber-Physical Systems and Internet of Things  
Room: Grand Ballroom 1-3



## Keynote: Approximate Computing for Energy-efficient Error-resilient Systems

**Time: 9:00 - 10:00 | Room: Grand Ballroom 1-3**

**Keynote Speaker:**

Kaushik Roy - *Purdue Univ.*

In today's world there is an explosive growth in digital information content. Moreover, there is also a rapid increase in the number of users of multimedia applications related to image and video processing, recognition, mining and synthesis. These facts pose an interesting design challenge to process digital data in an energy-efficient manner while catering to desired user quality requirements. Most of these multimedia applications possess an inherent quality of "error"-resilience. This means that there is considerable room for allowing approximations in intermediate computations, as long as the final output meets the user quality requirements. This relaxation in "accuracy" can be used to simplify the complexity of computations at different levels of design abstraction, which directly helps in reducing the power consumption. At the algorithm and architecture levels, the computations can be divided into significant and non-significant.

Significant computations have a greater impact on the overall output quality, compared to non-significant ones. Thus the underlying architecture can be modified to promote faster computation of significant components, thereby enabling voltage-scaling (at the same operating frequency). At the logic and circuit levels, one can relax Boolean equivalence to reduce the number of transistors and decrease the overall switched capacitance. This can be done in a controlled manner to introduce limited approximations in common mathematical operations like addition and multiplication.

All these techniques can be classified under the general topic of "Approximate Computing", which is the main focus of this talk.

### Biography:

Kaushik Roy received B.Tech. degree in electronics and electrical communications engineering from the Indian Institute of Technology, Kharagpur, India, and Ph.D. degree from the electrical and computer engineering department of the University of Illinois at Urbana-Champaign in 1990. He was with the Semiconductor Process and Design Center of Texas Instruments, Dallas, where he worked on FPGA architecture development and low-power circuit design. He joined the electrical and computer engineering faculty at Purdue University, West Lafayette, IN, in 1993, where he is currently Edward G. Tiedemann Jr. Distinguished Professor. His research interests include spintronics, device-circuit co-design for nano-scale Silicon and non-Silicon technologies, low-power electronics for portable computing and wireless communications, and new computing models enabled by emerging technologies. Dr. Roy has published more than 600 papers in refereed journals and conferences, holds 15 patents, supervised 70 PhD dissertations, and is co-author of two books on Low Power CMOS VLSI Design (John Wiley & McGraw Hill).

### Chair:

Jörg Henkel - *Karlsruhe Institute of Technology*

## CASES: Memory Management

**Time: 10:30 - 12:00 | Room: Marquis A**

### Chair:

Muhammad Shafique - *Karlsruhe Institute of Technology*

### 6.1 REDESIGNING A TAGLESS ACCESS BUFFER TO REQUIRE MINIMAL ISA CHANGES

Carlos Sanchez, Peter Gavin - *Florida State Univ.*

Daniel Moreau - *Chalmers Univ. of Technology*

Magnus Sjalander - *Norwegian Univ. of Science and Technology*

David Whalley - *Florida State Univ.*

Per Larsson-Edefors, Sally McKee - *Chalmers Univ. of Technology*

### 6.2 THRIFTY-MALLOC: A HW/SW CODESIGN FOR THE DYNAMIC MANAGEMENT OF HARDWARE TRANSACTIONAL MEMORY IN EMBEDDED MULTICORE SYSTEMS

Thomas Carle, Iris Bahar, Maurice Herlihy, Dimitra Papagiannopoulou - *Brown Univ.*

Tali Moreshet - *Boston Univ.*

Andrea Marongiu - *ETH Zurich*

### 6.3 FASTCOLLECT: OFFLOADING GENERATIONAL GARBAGE COLLECTION TO INTEGRATED GPU

Abhinav - *Indian Institute of Technology (BHU), Varanasi*

Rupesh Nasre - *IIT Madras*

## CODES + ISSS: Hungry for Power: Energy Efficiency in Heterogeneous Multiprocessors

**Time: 10:30 - 12:00 | Room: Marquis B**

### Chair:

Fadi Kurdahi - *Univ. of California, Irvine*

### Co-Chair:

Sudeep Pasricha - *Colorado State Univ.*

### 6.1 WEB BROWSER WORKLOAD CHARACTERIZATION FOR POWER MANAGEMENT ON HMP PLATFORMS

Nadja Peters, Sangyoung Park - *Technische Univ. München*

Samarjit Chakraborty - *TU Munich*

Hannes Payer, Benedikt Meurer, Daniel Clifford - *Google*

### 6.2 SPARTA: RUNTIME TASK ALLOCATION FOR ENERGY EFFICIENT HETEROGENEOUS MANY-CORES

Bryan Donyanavard - *Univ. of California at Irvine*

Tiago Muck - *Univ. of California, Irvine*

Santanu Sarma - *Univ. of California Irvine*

Nikil Dutt - *Univ. of California, Irvine*

### 6.3 ENERGY-EFFICIENT MAPPING OF REAL-TIME APPLICATIONS ON HETEROGENEOUS MPSOCS USING TASK REPLICATION

Jelena Spasic, Di Liu, Todor Stefanov - *Leiden Univ.*

## Special Session: IoT Day: Internet-of-Things: Key Enablers and Assistive Technologies

**Time: 10:30 - 12:00 | Room: City Center AB**

### Organizer:

Umit Ogras - *Arizona State Univ.*

Internet of things is perceived as the next big wave in computing. The success of this vision depends critically on our ability to design practical and secure systems that offer capabilities achievable using the existing computational infrastructure. This special session will address the practicality from an industrial perspective by discussing the industrial life-cycle of IoT devices, which emphasize reliability, resilience, safety, and security. It will delve deeper into the security aspects by demonstrating that a variety of affordable IoT products on the market usually suffer from resource limitations, which deem existing security mechanisms infeasible.

Finally, we will show that one of the areas that can be revolutionized by Internet of things is assistive technologies. We will present robust human-machine communication strategies that can provide access to IoT devices.

### 5SS.1 INDUSTRIAL IOT LIFECYCLE VIA DIGITAL TWINS

Arquimedes Canedo - *Siemens Corp.*

### 5SS.2 SECURITY AND PRIVACY CHALLENGES IN IOT-BASED MACHINE-TO-MACHINE COLLABORATIVE SCENARIOS

Pai Chou, Mohammad Al Faruque, Hsin Chung Chen - *Univ. of California, Irvine*

### 5SS.3 HUMAN-MACHINE COMMUNICATION FOR ASSISTIVE IOT TECHNOLOGIES

Alexandra Porter, Md Muztoba, Umit Y. Ogras - *Arizona State Univ.*

## EMSOFT: Autonomous Systems and their Verification

**Time: 10:30 - 12:00 | Room: Marquis C**

### Chair:

Aviral Shrivastava - *Arizona State Univ.*

### 7.1 INVITED EMBEDDED TUTORIAL: REQUIREMENT-BASED TESTING FOR EMBEDDED CONTROL SYSTEMS

Jyotirmoy Deshmukh - *Toyota Technical Center*

### 7.2 MODULAR DEDUCTIVE VERIFICATION OF SAMPLED-DATA SYSTEMS

Daniel Ricketts, Gregory Malecha, Sorin Lerner - *Univ. of California at San Diego*

### 7.3 THE SMT-BASED AUTOMATIC ROAD NETWORK GENERATION IN VEHICLE SIMULATION ENVIRONMENT

BaekGyu Kim, Akshay Jarandikar, Jonathan Shum, Shinichi Shiraishi, Masahiro Yamaura - *Toyota InfoTechnology Center*

## Special Session: CASES: Eastern Wisdom: Neuromorphic Computing Research in China

**Time: 14:00 - 15:30 | Room: Marquis A**

### Organizers:

Yiran Chen - *Univ. of Pittsburgh*

Hai (Helen) Li - *Univ. of Pittsburgh*

Neuromorphic computing, which stands for hardware acceleration of brain-inspired computation, has become one of the most active areas in computer engineering. In this session, we will introduce three representative works of neuromorphic computing research in China, including the innovative computer architecture, the ASIC accelerators, and the prototype built on emerging memristor technology

### 2SS.1 NEURAL NETWORK TRANSFORMATION AND CO-DESIGN UNDER NEUROMORPHIC HARDWARE CONSTRAINTS

Youhui Zhang, Yu Ji, Wenguang Chen - *Tsinghua Univ.*

Yuan Xie - *Univ. of California, Santa Barbara*

### 2SS.2 CAMBRICON: AN INSTRUCTION SET ARCHITECTURE FOR NEURAL NETWORKS

Zidong Du - *Chinese Academy of Sciences*

### 2SS.3 RRAM BASED LEARNING ACCELERATION

Yu Wang, Lixue Xia, Ming Cheng, Tianqi Tang, Boxun Li, Huazhong Yang - *Tsinghua Univ.*

## Special Session: CODES + ISSS: I am a Chip, Therefore: Can I Think? -- The Dawn of Self-Awareness in Cyber-Physical Systems

**Time: 14:00 - 15:30 | Room: Marquis B**

### Organizers:

Rolf Ernst - *Technische Univ. Braunschweig*

Fadi Kurdahi - *Univ. of California, Irvine*

Andreas Herkersdorf - *Technische Univ. München*

This session explores the current state-of-the-art and future directions for overhead-efficient self-aware HW/SW systems which guarantee critical properties such as real-time behavior, resilience, security, and energy efficiency. Unlike existing reactive systems whose specifications are fixed at design time, self-aware systems are proactive. This is critical for future cyber-physical systems which must be able to cope with scenarios that were not conceived when they were developed.

The first talk introduces the origins of self-awareness in psychology and its translation to computing systems. The second talk discusses self-awareness in heterogeneous multi-core systems and the “on-the-fly” computing. The third paper proposes an information processing factory model for cross-layer, self-aware platforms supporting cyber-physical systems.

The last paper builds on the concepts presented in the previous papers, presenting case studies derived from the Cyber-Physical Systems-on-Chip (CPSoC) platform, demonstrating self-awareness in dealing with complex interdependent metrics constraints, and managing cross-layer interactions in a mobile device.

### 6SS.1 TYPES OF COMPUTATIONAL SELF-AWARENESS AND HOW WE MIGHT IMPLEMENT THEM

Peter Lewis - *Univ. of Paderborn*

### 6SS.2 ON-THE-FLY COMPUTING: SELF-AWARE HETEROGENEOUS MULTI-CORES

Marco Platzner - *Univ. of Paderborn*

### 6SS.3 TOWARDS SYSTEM-LEVEL SELF-AWARENESS IN PREDICTABLE CYBER PHYSICAL COMPUTING PLATFORMS

Andreas Herkersdorf - *Technische Univ. München*

### 6SS.4 USING CROSS-LAYER SELF-AWARENESS TO COPE WITH DYNAMIC VARIABILITY IN PLATFORMS, ENVIRONMENTS, AND APPLICATIONS

Nikil Dutt - *Univ. of California, Irvine*

## EMSOFT: Formal Methods for Robust and Predictable Embedded Systems

*Time: 14:00 - 15:30 | Room: Marquis C*

**Chair:**

Florence Maraninchi - *Verimagic*

**8.1 INVITED EMBEDDED TUTORIAL: SYNTAX-GUIDED SYNTHESIS**

Rajeev Alur - *Univ. of Pennsylvania*

**8.2 PCFIRE: TOWARDS PROVABLE PREVENTATIVE CONTROL-FLOW INTEGRITY ENFORCEMENT FOR REALISTIC EMBEDDED SOFTWARE**

Jiaqi Tan, Hui Jun Tay, Utsav Drolia, Rajeev Gandhi, Priya Narasimhan - *Carnegie Mellon Univ.*

**8.3**

**A REFINEMENT THEORY FOR TIMED-DATAFLOW ANALYSIS WITH SUPPORT FOR REORDERING**

Joost Hausman - *Univ. of Twente*,  
Marco Bekooij - *Univ. of Twente + NXP Semiconductors*

## EMSOFT: Techniques for Real-Time Task and Communication Scheduling

*Time: 14:00 - 15:30 | Room: City Center AB*

**Chair:**

Björn Brandenburg - *Max Planck Institute for Software Systems*

**10.1 SCHEDULABILITY ANALYSIS OF MIXED-CRITICALITY SYSTEMS WITH MULTIPLE FREQUENCY SPECIFICATIONS**

Sanjoy Baruah - *Univ. of North Carolina, Chapel Hill*

**10.2**

**ON-THE-FLY FAST OVERRUN BUDGETING FOR MIXED-CRITICALITY SYSTEMS**

Biao Hu - *Tech. Univ. Muenchen*  
Kai Huang - *Sun Yat-sen Univ.*  
Pengcheng Huang - *ETH Zurich*  
Lothar Thiele - *Swiss Federal Institute of Technology Zurich*  
Alois Knoll - *Tech. Univ. Muenchen*

**10.3**

**SYNTHESIZING TIME-TRIGGERED SCHEDULES FOR SWITCHED NETWORKS WITH FAULTY LINKS**

Guy Avni - *IST Austria*  
Shibashis Guha - *Hebrew Univ.*  
Guillermo Rodriguez-Navas - *Malardalen Univ.*

## CODES + ISSS: Energy-Aware Embedded System Architectures

*Time: 16:00 - 17:30 | Room: Marquis A*

**Chair:**

Yiran Chen - *Univ. of Pittsburgh*

**Co-Chair:**

Umit Ogras - *Arizona State Univ.*

**5.1 CHECKPOINT AWARE HYBRID CACHE ARCHITECTURE FOR NV PROCESSOR IN ENERGY HARVESTING POWERED SYSTEMS**

Mimi Xie - *Oklahoma State Univ.*  
Mengying Zhao - *Shandong Univ.*  
Chen Pan - *Oklahoma State Univ.*  
Hehe Li, Yongpan Liu - *Tsinghua Univ.*  
Youtao Zhang - *Univ. of Pittsburgh*,  
Chun Jason Xue - *City Univ. of Hong Kong*  
Jingtong Hu - *Oklahoma State Univ.*

**5.2**

**NANO-ENGINEERED ARCHITECTURES FOR ULTRA-LOW POWER WIRELESS BODY SENSOR NODES**

Rubén Braojos - *École Polytechnique Fédérale de Lausanne*  
Tony F. Wu - *Stanford Univ.*  
Giovanni Ansaloni - *USI - Lugano*,  
Mohamed M. Sabry - *Stanford Univ.*  
David Atienza - *École Polytechnique Fédérale de Lausanne*  
Subhasish Mitra, H.-S. Philip Wong - *Stanford Univ.*

**5.3**

**MITIGATION OF HOMODYNE CROSSTALK NOISE IN SILICON PHOTONIC NOC ARCHITECTURES WITH TUNABLE DECOUPLING**

Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha - *Colorado State Univ.*

## CODES + ISSS: Acceleration of Analytic Workloads

**Time: 16:00 - 17:30 | Room: Marquis B**

**Chair:**

Houman Homayoun - *George Mason Univ.*

**Co-Chair:**

Mohammad Al Faruque - *Univ. of California, Irvine*

**7.1 ASYNCSTRIPE: I/O EFFICIENT ASYNCHRONOUS GRAPH COMPUTING ON A SINGLE SERVER**

ShuHan Cheng, Guangyan Zhang, Jiwu Shu, Weimin Zheng - *Tsinghua Univ.*

**7.2 ZERO AND DATA REUSE-AWARE FAST CONVOLUTION FOR DEEP NEURAL NETWORKS ON GPU**

Hyunsun Park - *Pohang Univ. of Science and Technology*  
Dongyoung Kim, Junwhan Ahn, Sungjoo Yoo - *Seoul National Univ.*

**7.3 RUNTIME CONFIGURABLE DEEP NEURAL NETWORKS FOR ENERGY-ACCURACY TRADE-OFF**

Hokchhay Tann, Soheil Hashemi, R. Iris Bahar, Sherief Reda - *Brown Univ.*

## EMSOFT: Management of Flash-Based and Hybrid Memory Systems for Improved Latency, Lifetime, and Reliability

**Time: 16:00 - 17:30 | Room: Marquis C**

**Chair:**

Binoy Ravindran - *Virginia Polytechnic Institute and State Univ.*

**9.1 I/O SCHEDULING WITH MAPPING CACHE AWARENESS FOR FLASH BASED STORAGE SYSTEMS**

Cheng Ji, Chao Wu - *City Univ. of Hong Kong*  
Li-Pin Chang - *National Chiao Tung Univ.*  
Liang Shi - *Chongqing Univ.*  
Jason Xue - *City Univ. of Hong Kong*

**9.2 THE DESIGN OF AN EFFICIENT SWAP MECHANISM FOR HYBRID DRAM-NVM SYSTEMS**

Xianzhang Chen - *Chongqing Univ.*  
Edwin H.-M. Sha - *Univ. of Texas at Dallas*  
Weiwen Jiang, Qingfeng Zhuge, Junxi Chen, Jiejie Qin, Yuansong Zeng - *Chongqing Univ.*

**9.3 A FAST, LIGHTWEIGHT, AND RELIABLE FILE SYSTEM FOR WIRELESS SENSOR NETWORKS**

Biswajit Mazumder - *Clemson Univ.*  
Jason Hallstrom - *Florida Atlantic Univ.*

## Best Paper Awards Ceremony & ESWEEK Panel - Embedded Systems Challenges in the Era of Cyber-Physical Systems and Internet of Things

**Time: 18:00 - 19:30 | Room: Grand Ballroom 1-3**

**Organizers:**

Tei-Wei Kuo - *National Taiwan Univ.*  
Chenyang Lu - *Washington Univ.*

We are in the midst of an exciting transformation from traditional embedded systems to cyber-physical systems (CPS) and Internet-of-Things (IoT). How should the embedded systems community respond to new challenges arising from CPS and IoT? In this panel, leaders and experts with diverse backgrounds will discuss new research opportunities and directions to address fundamental requirements of CPS and IoT, such as autonomy, dependability, security and scalability.

**Moderator:**

Yiran Chen - *Univ. of Pittsburgh*

**Panelists:**

Chenyang Lu - *Washington Univ.*  
Gang Qu - *Univ. of Maryland*  
Raj Rajkumar - *Carnegie Mellon Univ.*  
David Corman - *National Science Foundation*  
Christopher Martin - *Bosch Research and Technology Center*



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# WORKSHOPS & SYMPOSIA SCHEDULE

## **AC'16:** Workshop on Approximate Computing

*Thursday, October 6 | Time: 8:00 - 18:00 | Room: Grand Ballroom Salon 3*

## **CAIRES'16:** 1st Workshop on Collaboration of Academia and Industry for Real World Embedded Systems

*Thursday, October 6 | Time: 8:00 - 18:00 | Room: Marquis B*

## **CyPhy'16:** 6th Workshop on Design, Modeling and Evaluation of Cyber Physical Systems

*Thursday, October 6 | Time: 8:00 - 18:00 | Room: Grand Ballroom Salon 2*

## **EWiLi'16:** 6th Embedded Operating System Workshop

*Thursday, October 6 | Time: 8:00 - 18:00 | Room: Grand Ballroom Salon 1*

## **HILT'16:** ACM SIGAda's High Integrity Language Technology International Workshop on Model-Based Development and Contract-Based Programming

*Thursday, October 6 - Friday, October 7 | Time: 8:00 - 18:00 | Room: City Center A*

## **WESE'16:** Workshop on Embedded and Cyber-Physical Systems Education

*Thursday, October 6 | Time: 8:00 - 18:00 | Room: City Center B*

## **RSP Symposium:** IEEE International Symposium on Rapid System Prototyping

*Thursday, October 6 - Friday, October 7 | Room: Marquis C*

## **ESTIMedia Symposium:** 14th IEEE Symposium on Embedded Systems for Real-time Multimedia

*Thursday, October 6 - Friday, October 7 | Room: Marquis A*



## AC'16: Workshop on Approximate Computing

Thursday, October 6 | Time: 8:00 - 18:00 | Room: Grand Ballroom Salon 3

Approximate Computing exploits the inherent error resilience of many applications to optimize power consumption, run time, and/or chip area. In particular in audio, image and video processing, but also in machine learning, data mining or analytics, approximate results are “good enough” and hard to distinguish from perfect results. In the past few years, approximate computing has been addressed from various directions. Promising solutions range from approximate arithmetic units over dedicated micro-architectures to special language constructs and compilers. The goal of the workshop is to provide an interdisciplinary forum for presenting and discussing scientific results, emerging ideas, applications, hot topics and new trends in the area of Approximate Computing.

### Organizers:

#### General Chairs:

Sybille Hellebrand, Paderborn Univ., Germany

Hans-Joachim Wunderlich, Stuttgart Univ., Germany

#### Steering Committee:

Jie Han, Univ. of Alberta, Canada

Sybille Hellebrand, Paderborn Univ., Germany

Jörg Henkel, KIT, Germany

Anand Raghunathan, Purdue Univ., Germany

Kaushik Roy, Purdue Univ., USA

Adit Singh, Auburn Univ., USA

Hans-Joachim Wunderlich, Stuttgart Univ., Germany

### Program Committee:

Alberto Bosio, LIRMM, France

Hadi Esmaeilzadeh, Georgia Tech, USA

Nam Sung Kim, Univ. of Illinois, Urbana Champaign, USA

Marco Platzner, Paderborn Univ., Germany

Christian Plessl, Paderborn Univ., Germany

Lukas Sekanina, Brno Univ., Czech Republic

Mehdi Tahoori, KIT, Germany

Jürgen Teich, Erlangen-Nuremberg Univ., Germany

Norbert Wehn, TU Kaiserslautern, Germany

Heike Wehrheim, Paderborn Univ., Germany

Qiang Xu, Chinese Univ. of Hong Kong



## AC'16: Workshop on Approximate Computing

Thursday, October 6 | Time: 8:00 - 18:00 | Room: Grand Ballroom Salon 3

### AC'16 PROGRAM

#### 9:00 – 10:00 Opening and Keynote

Chair: Hans-Joachim Wunderlich

Sybille Hellebrand. Opening Address

Keynote: To be announced

#### 10:00 - 10:30 Coffee and Posters

M. Ammar Ben Khadra, Dominik Stoffel and Wolfgang Kunz. Approximate Computing: Facing The Control Flow

Mario Barbareschi, Domenico Amelino, Antonino Mazzeo and Alberto Bosio. Towards Approximate Computing Applications by Employing Mutation Code Approach

Gabriel Paillard, Rubens Almeida, Rui Mello Junior and Felipe França. The Gamma multiset rewriting paradigm: a parallel approximate computing framework

Ankit Mondal and Ankur Srivastava. Data Driven Optimizations for MTJ based Stochastic Computing

Stephen Jeffress, Tim Palmer and Peter Duben. Weather and Climate Simulations with Approximate Computing

#### 10:30 – 12:30 Session 1: Multi-Level Design and Test

Chair: Jörg Henkel

Seogoo Lee, Lizy K. John and Andreas Gerstlauer. Data Dependent Loop Approximation Technique in High-Level Synthesis

Georgios Zervakis, Sotirios Xydis, Vasileios Tsoutsouras, Dimitrios Soudris and Kiamal Pekmestzi. Multi-Level Approximation for Inexact Accelerator Synthesis Under Voltage Island Constraints

Alexander Schöll, Claus Braun and Hans-Joachim Wunderlich. Hardware/Software Co-Characterization for Approximate Computing

Imran Wali, Arnaud Virazel, Patrick Girard, Mario Barbareschi and Alberto Bosio. A Case Study on the Approximate Test of Integrated Circuits

#### 12:30 – 14:00 Lunch

#### 14:00 – 15:30 Session 2: Near Memory Computing and Deep Learning

Chair: TBD

Amir Yazdanbakhsh, Choungki Song, Pejman Lotfi-Kamran, Hadi Esmailzadeh, Nam Sung Kim and Jake Sacks. NAX: Near Data Approximate Computing

Hokchhay Tann, Soheil Hashemi, Iris Bahar and Sherief Reda. Approximate Computing in Deep Neural Networks

Chi-Sheng Daniel Shih, Chang-Min Yang, Chun-Yo Lin, Pei-Kuei Tsung and Roy Ju. Using deep learning and imprecise computation for safety critical applications

#### 15:30 – 16:00 Coffee

#### 16:00 – 17:30 Session 3: Applications

Chair: TBD

Anca Molnos, Yves Durand and Nicolas Gonther. Trading sharpness with energy consumption in a lens autofocus application

Jochen Rust and Steffen Paul. Numeric Function Approximation with Separate Accuracy Domains

James Davis, Joshua Levine, Edward Stott, Peter Cheung, George Constantinides, Charlie Leech, Domenico Balsamo, Michael Lass, Thomas D. Kühne and Christian Plessl. Using Approximate Computing in Scientific Codes

## CAIRES'16: 1st Workshop on Collaboration of Academia and Industry for Real World Embedded Systems

Thursday, October 6 | Time: 8:00 - 18:00 | Room: Marquis B

### Organizers:

Rolf Ernst - *Technische Univ. Braunschweig*  
Marco Di Natale - *Scuola Superiore Sant'Anna*  
Sascha Uhrig - *Airbus S.A.S.*  
Sophie Quinton - *Inria Grenoble - Rhône-Alpes*  
Devendra Rai - *Bosch Research*

The objective of the first workshop on the "Collaboration of Academia and Industry for Real World Embedded Systems" (or, CAIRES) is to bring together experts from academia and the industry in a collaboration for the design and implementation of industrial strength embedded systems. The workshop will focus on the two most important aspects of such a collaboration.

(1). Challenges in the transfer of appropriate and formalized problem statements from industry to academia; (2). Challenges in the transfer of methods and tools developed by the academia back to the industry, including methods to establish necessary quality control over methods and tools, e.g. using existing or new benchmarks.

The workshop will have two parts:

### Talks:

Carefully selected speakers from academia and industry will share both negative and positive experiences as well as case-studies relating to the triple challenges listed above.

### Break-out Session:

Depending on participation, and interest, an interactive session wherein academics and industrialists will be organized in small groups, with each group focusing on one of the following: (a) formalize an interesting industrial problem for research, (b) formalizing specifications for methods and tools, or (c) setting up new benchmarks for industrial embedded systems.

### Speakers:

Arne Hamann - *Bosch Research*  
Dirk Ziegenbein - *Bosch Research*  
Rainer Leupers - *RWTH Aachen Univ.*  
Jim Kapinski - *Toyota Motor Corp.*  
Alexandre Esper - *Critical Software*  
Bjoern Brandenburg - *Max Planck Institute for Software Systems*  
Arvind Easwaran - *Nanyang Technological Univ.*  
Zaykov Pavel - *Honeywell International Inc.*





## CyPhy'16: Sixth Workshop on Design, Modeling and Evaluation of Cyber Physical Systems

*Thursday, October 6 | Time: 8:00 - 18:00 | Room: Grand Ballroom Salon 2*

The workshop brings together researchers and practitioners working on modeling, simulation, and evaluation of Cyber Physical Systems (CPSs), based on a broad interpretation of these areas, to collect and exchange expertise from a diverse set of disciplines. The workshop places particular focus on techniques and components to enable and support virtual prototyping and testing. Topics of interest include CPS aspects pertaining to foundations; methods; case studies and tools.

### **Organizers:**

#### **General Chair:**

Walid Taha, Halmstad & Rice Universities

#### **Program Chairs:**

Christian Berger, Chalmers and Univ. of Gothenburg

Mohammad Reza Mousavi, Halmstad Univ.

Rafael Wisniewski, Aalborg U. Denmark

#### **Program Committee:**

Jakob Axelsson, SICS and Mälardalen Univ.

Christian Berger, Chalmers and Univ. of Gothenburg

Manuela Bujorianu, Leicester Univ.

Thao Dang, Verimag, France

Georgios Fainekos, Arizona State Univ.

Scott Hissam, Carnegie Mellon Univ.

Daisuke Ishii, Tokyo Institute of Technology

Mehdi Kargahi, Univ. of Tehran

Zhiyun Lin, Zhejiang Univ.

Mohammad Reza Mousavi, Halmstad Univ.

Wojciech Mostowski, Halmstad Univ.

Enrico Pagello, Univ. of Padua, Italy

Mihaly Petreczky, CNRS Lille, France

Michel Reniers, Eindhoven Univ. of Technology

Bernhard Rumpe, RWTH Univ. Aachen

Maytham Safar, Kuwait Univ.

Bernhard Schätz, TU München

Christoph Seidl, TU Braunschweig

Christoffer Sloth, Aalborg Univ.

Jonathan Sprinkle, Univ. of Arizona

Martin Steffen, Oslo Univ.

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Walid Taha, Halmstad & Rice Universities



## CyPhy'16: Sixth Workshop on Design, Modeling and Evaluation of Cyber Physical Systems

Thursday, October 6 | Time: 8:00 - 18:00 | Room: Grand Ballroom Salon 2

### CYPHY'16 PROGRAM

#### 08:30-09:00 Registration

#### 09:00-10:00 (Keynote)

Jyotirmoy Deshmukh, Toyota Technical Center  
Formal methods for cyberphysical systems in the automotive domain

#### 10:00-10:30 Coffee / tea break

#### 10:30-12:30

Ken Vanherpen, Joachim Denil, Paul De Meulenaere and Hans Vangheluwe. Ontological Reasoning as an Enabler of Contract-Based Co-Design.

Waheed Ahmad, Bugra Mehmet Yildiz, Arend Rensink and Marielle Stoelinga. A Model-Driven Framework for Hardware-Software Co-design of Dataflow Applications.

Sebastian Schlesinger, Paula Herber, Thomas Göthel and Sabine Glesner. Proving Correctness of Refactorings for Hybrid Simulink Models with Control Flow.

Kenichi Betsuno, Shota Matsumoto and Kazunori Ueda. Symbolic Analysis of Hybrid Systems Involving Numerous Discrete Changes Using Loop Detection.

#### 12:30-14:00 Lunch

#### 14:00-15:30

Georgiana Caltais, Florian Leitner-Fischer, Stefan Leue and Jannis Weiser. SysML to NuSMV model transformation via object-orientation.

Stefan Schwab, Bern Holzmueller and Soeren Hohmann. Automated Verification of Switched Systems using Hybrid Identification.

Jonas Westman, Mattias Nyberg and Oscar Thyden. CPS Specifier -- A Specification Tool for Safety-Critical Cyber-Physical Systems.

#### 15:30-16:00 Coffee / tea break

#### 16:00-17:00

Shafiul Azam Chowdhury, Taylor Johnson and Christoph Csallner. CyFuzz: A Differential Testing Framework for Cyber-Physical Systems Development Environments.

Fergus Leahy and Naranker Dulay. Ardan: Using 3D Game Engines in Cyber-Physical Simulations.



## **EWiLi'16: Sixth Embedded Operating System Workshop**

**Thursday, October 6 | Time: 8:00 - 18:00 | Room: Grand Ballroom Salon 1**

### **Organizers:**

Jalil Boukhobza - *Univ. européenne de Bretagne*

Marco Dominico Santambrogio - *Polytechnic Univ. of Milan*

Frank Singhoff - *Univ. européenne de Bretagne*

Giuseppe Lipari - *Univ. Lille*  
Duo Liu - *Chongqing Univ.*

EWiLi'16, the 6th Embedded Operating System Workshop, aims at presenting state-of-the-art research, experimentations, significant and original realizations that focus on the design and implementation of embedded operating systems in both academic and industrial worlds.

The EWiLi workshop is embedded operating system centric and includes but is not limited to the following topics:

- Embedded operating systems and education
- Methods, software and tool chains
- Model-driven engineering and embedded operating systems
- Data management and memory hierarchy optimization
- Real-time, concurrency, scheduling and temporal performance

- File systems, storage, and I/Os in embedded operating systems
- Embedded operating systems and reconfigurable architectures
- Embedded operating systems and MPSOC
- Embedded operating systems and multi-core
- Embedded operating systems and sensor networks
- Energy and power optimization in embedded operating systems
- Debugging and profiling for embedded operating systems
- Case studies and application projects
- Performance evaluation and optimization

This is the second edition of the workshop to be held in conjunction with the Embedded Systems Week (ESWEEK) in Pittsburgh (US), after the 2015 edition in Amsterdam, The Netherlands. The previous editions were organized in Lisbon/Portugal (2014), Toulouse/France (2013), Lorient/France (2012), and Saint Malo/France (2011).

### **Invited Speaker:**

Daniel Mossé - *Univ. of Pittsburgh*





## **HILT'16: ACM SIGAda's High Integrity Language Technology International Workshop on Model-Based Development and Contract-Based Programming**

**Thursday, October 6 - Friday, October 7 | Time: 8:00 - 18:00 | Room: City Center A**

### **Chairs:**

Julien Delange - *Carnegie Mellon Univ.*  
Tucker Taft - *AdaCore*

### **Organizers:**

David Cook - *Stephen F. Austin State Univ.*  
Dirk Craeynest - *Katholieke Univ. Leuven*  
Clyde Roby - *Institute for Defense Analyses*  
Alok Srivastava - *Engility Corporation*  
Ricky E. Sward - *MITRE Corporation*

The HILT 2016 Workshop is focused on the synergy between Model-Based Development and Contract-Based Programming, producing a formal model-driven approach to the development of high-assurance software-intensive systems. An important output of this formal model-driven approach is code that preserves explicit representations, in the form of contracts (such as pre- and post-conditions), of the safety and security requirements of the software. This depends on having formalized representations of at least some of the high-level requirements of the system, and allows for consistency checks and assurance case evaluation at every level of development, from the high-level architecture, through the coding and testing of the individual software components of the system. This formal approach also enables verification of system requirements and consistency throughout the integration of the components to physically build the system.

The HILT 2016 Workshop will provide a forum for communities of researchers and practitioners from academic, industrial, and governmental settings, to come together, share experiences, and forge partnerships focused on integrating and deploying tool and language combinations to support a formal approach to model-based development. The workshop will be a combination of presentations and panel discussions, with one or more invited speakers.

Workshop Sponsor- ACM SIGAda

Corporate Sponsors- AdaCore, Inc. and ANSYS, Inc.



# THURSDAY, OCTOBER 6

## **HILT'16: ACM SIGAda's High Integrity Language Technology International Workshop on Model-Based Development and Contract-Based Programming**

*Thursday, October 6 - Friday, October 7 | Time: 8:00 - 18:00 | Room: City Center A*

### **THURSDAY 6-OCTOBER-2016**

**9:00-9:10am** -- *Welcome and logistics*

**9:10-9:50am** -- *John Knight, Univ. of Virginia, keynote*

**9:50-10:00am** -- *Q&A*

**10:00-10:30am** -- *Break*

**10:30am-12:30pm** -- *Session*

Static Analysis of Complex Systems (Part I)

**12:30-2:00pm** -- *Lunch*

**2:00-3:00pm** -- *Session*

Static Analysis of Complex Systems (Part II)

**3:00-3:30pm** -- *Showcase*

Static Analysis and Model Checking Tools (Part I)

**3:30-4:00pm** -- *Break*

**4:00-5:30pm** -- *Showcase*

Static Analysis and Model Checking Tools (Part II)

**6:30pm-9:00pm** -- *Social Event*

Bernard Dion -- Dinner speaker

### **FRIDAY 7-OCTOBER-2016**

**9:00-9:45am** -- *Phil Koopman, Carnegie Mellon Univ., Keynote*

**9:45-10:00** -- *Q&A*

**10:00-10:30** -- *Break*

**10:30-11:30** -- *Session*: Simulation and Dynamic Analysis of Complex Systems

**11:30-12:30** -- *Showcase*: Simulation, Testing, and Debugging Tools (Part I)

**12:30-1:30pm** -- *Lunch*

**1:30pm-3:00pm** - *Showcase*: Simulation, Testing, and Debugging Tools (Part II)

**3:00 - 3:30** -- *Break*

**3:30 - 5:00** -- *Panel*: Modeling and Simulation of Complex Systems



## **WESE'16: Workshop on Embedded and Cyber-Physical Systems Education**

**Thursday, October 6 | Time: 8:00 - 18:00 | Room: City Center B**

### **Organizers:**

Martin Torngrén - *Royal Institute of Technology*

Martin Grimheden - *Royal Institute of Technology*

Falk Salewski - *Münster Univ. of Applied Sciences*

Educating and continued training of engineers is of increasing importance given the expanding role of embedded and cyber-physical systems in our society. WESE brings researchers, educators, and industrial representatives together to assess needs and share design, research, and experiences in embedded and cyber-physical systems education. WESE 2016 is the 11th workshop in this series (for more info, see here: <http://www.emsig.net/conf/2016/wese/>).

### **Keynotes:**

*A Recent History of Hardware and Software Development and Its Impact on Embedded Systems Education*

Jeff Jackson, Univ. of Alabama

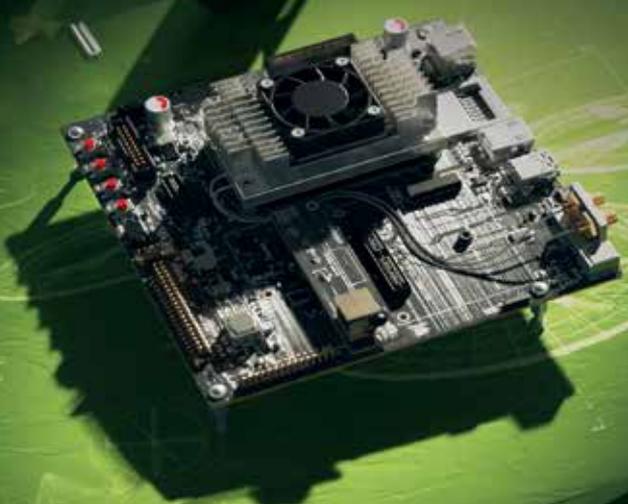
In this presentation we will review a history of computer hardware and software development over the past thirty years and note impacts of these changes on embedded systems education. We will examine evolving standards for hardware and software design and consider the impact of these changes on both technological and pedagogical approaches to embedded systems education.

We will note the various demands both hardware and software technological improvements have made on the embedded systems body-of-knowledge and present some possible road maps for student embedded systems education in the next decade. This will include hardware, software and programming language innovations impacting the field.

*An Industrial Perspective to Cyber-Physical Workforce Training*

William P. Milam, Ford Motor Company

Industry consumes students. We hire graduates and put them to work developing new products, enhancing existing products and supporting older products. The role they will take on depends on their education, experience and interest. For this talk we want to focus on the first two; education and experience. Are they majoring in a traditional engineering program? Computer Science? What is their minor? Have they worked in teams? Are they able to work collectively across engineering domains? These are especially important criteria in consumer facing industries, such as automotive, where time to market, reliability and cost are major factors.

A top-down view of an NVIDIA Jetson TX1 Developer Kit. The board is populated with various components including a central processor with a cooling fan, RAM modules, and various connectors. It is set against a dark green background with faint, glowing green lines and patterns, suggesting a high-tech or AI environment.

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# RSP SYMPOSIUM

**THURSDAY OCT 6, 2016**

**8:50 – (10 mins) Symposium Opening**

**Session 1 – Keynote**

9:00 – (60 mins) Keynote: Rethinking Memory System Design - Onur Mutlu - ETH Zurich

**10:00 – Coffee**

**Session 2 – Invited Talks: Virtualization and Visualization**

10:30 – (30 mins) Invited Paper: Embedded Virtualization for the Design of Secure IoT Applications  
C. Moratelli, S. Filho and F. Hessel - PUCRS

11:00 – (30 mins) Invited Paper: MORPh: Mobile OLED Power Friendly Camera System  
Xiang Chen, Jiachen Mao, Jiafei Gao, Kent Nixon, and Yiran Chen – Univ. of Pittsburgh

**Session 3 – Embedded Systems for Medical Applications**

11:30 – (30 mins) A HW/SW Embedded System for Accelerating Diagnosis of Glaucoma From Eye Fundus Images  
Paulo Cezar Dantas Junior, Andrea Sarmento and Adriano Sarmento - Centro de Informatica Universidade Federal de Pernambuco and Clinica Oftalmologica Zona Sul

12:00 – (30 mins) EEGu2: An Embedded Device for Brain/Body Signal Acquisition and Processing  
Shen Feng, Mian Tang, Fernando Quivira, Tim Dyson, Filip Cuckov and Gunar Schirner – Northeastern Univ. and Univ. of Massachusetts Boston

**12:30 – Lunch**

**Session 4 – Performance and Prototyping with FPGAs**

14:00 – (30 mins) Automatic Detection and Elision of Reset Sub-Circuits  
Panagiotis Patros and Kenneth Kent – Univ. of New Brunswick

14:30 – (30 mins) Architectural Performance Analysis of FPGA Synthesized LEON Processors  
Corentin Damman, Gregory Edison, Fabrice Guet, Eric Noulard, Luca Santinelli and Jerome Hugues – Institute for Space and Aeronautics Engineering (ISAE) and ONERA (The French Aerospace Lab)

15:00 – (30 mins) On-Board Non-Regression Test of HLS Tools Targeting FPGA  
Arief Wicaksana, Adrien Prost-Boucle, Olivier Muller, Arif Sasongko and Frédéric Rousseau - Laboratoire TIMA and STEI - Institut Teknologi Bandung

**15:30 – Coffee**

**Session 5 – Real-time**

16:00 – (30 mins) Invited Paper: On platforms for CPS - adaptive, predictable and efficient  
Lothar Thiele, Felix Sutton, Romain Jacob, Reto da Forno and Jan Beutel – ETH Zurich

16:30 – (30 mins) Overloads in Compositional Embedded Real-Time Control Systems  
Akramul Azim – Univ. of Ontario Institute of Technology

17:00 – (30 mins) Efficient Parallel Multi-Objective Optimization for Real-time Systems Software Design Exploration  
Rahma Bouaziz, Laurent Lemarchand, Frank Singhoff, Bechir Zalila and Mohamed Jmaiel - Univ. of Sfax, Univ. of Bretagne Occidentale and Digital Research Center of Sfax

17:30 – (15 mins) Design of an Expandable Real-time Simulation (eRTS) Platform for Multi-level Rapid Prototyping  
Ankurkumar Patel, Troy Silloway, Fnu Qinggele and Yong-Kyu Jung - Gannon Univ. and GE Transportation

17:45 – (15 mins) Architecture Exploration of Intelligent Robot System using ROS-compliant FPGA Component  
Takeshi Ohkawa, Kazushi Yamashina, Takuya Matsumoto, Kanemitsu Ootsu and Takashi Yokota – Utsunomiya Univ.

**18:00 – End of day**



# RSP SYMPOSIUM

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**FRIDAY OCT 7, 2016**

**Session 6 – System-on-Chip Prototyping and Simulation**

9:00 - (30 mins) Rapid SoC Prototyping Utilizing Quilt Packaging Technology For Functional Block Partitioning

Tian Lu, Jason Kulick and Carlos Ortega – Indiana Integrated Circuits

9:30 - (30 mins) RapidSoC: Short Turnaround Creation of FPGA Based SoCs

Jakob Wenzel and Christian Hochberger - Technische Universität Darmstadt

**10:00 – Coffee**

**Session 7 – Exploration and Design of Systems**

10:30 – (30 mins) Simulation driven insertion of data prefetching instructions for early software-on-SoC optimization

Perrin Njoyah Ntafam, Eric Paire, Alain Clouard and Frédéric Petrot – STMicroelectronics and Univ. Grenoble Alpes, TIMA

11:00 - (30 mins) HAMEX: Heterogeneous Architecture and Memory Exploration framework

Kasra Moazzemi, Roger Chen-Ying Hsieh and Nikil Dutt – Univ. of California, Irvine

11:30 - (30 mins) Inter-FPGA Routing Environment for Performance Exploration of Multi-FPGA Systems

Umer Farooq, Roselyne Chotin-Avot, Habib Mehrez and Moazzam Azeem - Universite Pierre et Marie Curie (UPMC)

**Session 7 – Exploration and Design of Systems**

12:00 - (15 mins) Model-driven Design & Synthesis of the SHA-256 Cryptographic Hash Function in ReWire  
William Harrison, Adam Procter and Gerard Allwein – Univ. of Missouri and US Naval Research Laboratory

12:15 - (15 mins) Schedulability-Guided Exploration of Multi-core Systems

Rabeh Ayari, Imane Hafnaoui, Giovanni Beltrame and Gabriela Nicolescu - Ecole Polytechnique de Montreal

12:30 - (15 mins) Transforming VHDL Descriptions into Formal Component-based Models

Ayoub Nouri, Rahma Benatitallah, Anca Molnos, Christian Fabre, Frederic Heitzmann and Olivier Debicki – CEA Leti

**12:45 – Symposium Closing**



# ESTIMEDIA SYMPOSIUM

## Technical Program | ESTIMedia 2016

THURSDAY OCT 6, 2016

### [08:30 – 09:00] Opening

TPC Co-Chairs: Muhammad Shafique, Vienna Univ. of Technology (TU Wien), Austria, and Sander Stuijk, TU Eindhoven, The Netherlands

### [09:00 – 10:00] Keynote – 1

Title: To Be Announced

Speaker: Vinod Kathail, Xilinx [Tentative Confirmation]

Session Chair: Muhammad Shafique, Vienna Univ. of Technology (TU Wien), Austria

### [10:00 – 10:30] Coffee Break

#### [10:30 – 12:30] Special Session 1:

#### “Implementation of Deep Neural Networks and Its Applications”

Each Talk Slot is of 30 Mins. (25 mins. Presentation + 5 mins. Q&A)

Organizer and Session Chair: Yiran Chen, Univ. of Pittsburgh, USA

Talk 1 – Efficient Neural Computing using Cellular Array of Magneto-Metallic Neurons and Synapses

Speaker: Kaushik Roy, Purdue Univ., USA

Talk 2 – Reflections of Deep Networks in Multimedia: From an Industry Perspective

Speaker: Liangliang Cao, Yahoo Labs, USA

Talk 3 – Real-Time Pedestrian Detection with Convolutional Neural Network on Customized Hardware

Speaker: Yu Wang, DeePhi Tech. and Tsinghua Univ., China

Talk 4 – An Efficient Deep Convolutional Network Architecture for Road Scene Understanding

Speaker: Yiran Chen, Univ. of Pittsburgh, USA

### [12:30 – 13:30] Lunch Break

#### [13:30 – 14:30] Industrial Sky Talk

Title: Embedded Deep Learning

Speaker: Soumith Chintala, Facebook, USA

Session Chair: Muhammad Shafique, Vienna Univ. of Technology (TU Wien), Austria

#### [14:30 – 15:30] Technical Session 1: “Mobile Multimedia for Healthcare and Internet-of-Things”

Each Talk Slot is of 20 Mins. (18 mins. Presentation + 2 mins. Q&A)

Session Chair: Hyunok Oh, Hanyang Univ., Korea

Talk 1 – Mobile Ultrasound Imaging on Heterogeneous Multi-Core Platforms

Authors: Andreas Kurth, Andreas Tretter, Pascal Alexander Hager, Sergio Sanabria, Orçun Göksel, Lothar Thiele and Luca Benini

Talk 2 – GigE Vision Data Acquisition for Visual Servoing using SG/DMA Proxying

Authors: Martin Geier, Florian Pitzl and Samarjit Chakraborty

Talk 3 – Rapid Precedent-Aware Pedestrian and Car Classification on Constrained IoT Platforms

Authors: Jay Danner, Linda Wills, Elbert M. Ruiz and Lee W. Lerner

#### [15:30 – 16:00] Poster Discussion and Coffee Break

#### [16:00 – 17:00] Technical Session 2: “Efficient Resource Management for Multimedia Systems”

Each Talk Slot is of 20 Mins. (18 mins. Presentation + 2 mins. Q&A)

Session Chair: Petru Eles, Linköping Univ., Sweden

Talk 1 – Multi-Path Scheduling for Multimedia Traffic in Real-Time On-chip Network

Authors: Adam Kostrzewa, Selma Saidi and Rolf Ernst

Talk 2 – Resource Aggregation for Collaborative Video from Multiple Projector enabled Mobile Devices

Authors: Hung Nguyen, Fadi Kurdahi and Aditi Majumder

Talk 3 – On Detecting and Using Memory Phases in Multimedia Systems

Authors: Hossein Tajik, Bryan Donyanavard and Nikil Dutt

#### [17:00 – 17:30] Poster Discussion and Coffee Break



# ESTIMEDIA SYMPOSIUM

**FRIDAY OCT 7, 2016**

**[08:00 – 10:00] Special Session 2: “Power-Thermal Efficiency and Self-Awareness in Mobile Multimedia Devices”**

Each Talk Slot is of 30 Mins. (25 mins. Presentation + 5 mins. Q&A)

Organizer and Session Chair: Muhammad Shafique, Vienna Univ. of Technology (TU Wien), Austria

Talk 1 – Dynamic Power Management in Mobile Systems: Opportunities and Challenges

Speaker: Raid Ayoub with Michael Kishinevsky, Intel, USA

Talk 2 – Towards Self-Aware Mobile Multimedia Systems through Intelligent Cross-Layer Coordination

Speaker: Fadi Kurdahi with Nikil Dutt, Univ. of California Irvine (UCI), USA, and Axel Jantsch, Vienna Univ. of Technology (TU Wien), Austria

Talk 3 – Providing Sustainable Performance in Thermally Constrained Mobile Devices

Speaker: Ayse K. Coskun with Onur Sahin, Boston Univ., USA

Talk 4 – To Be Announced

Speaker: Sherief Reda with Kapil Dev, Brown Univ., USA

**[10:00 – 10:30] Coffee Break**

**[10:30 – 11:30] Keynote – 2**

Title: ThirdEye: Visual Assist for Grocery Shopping

Speaker: Vijaykrishnan Narayanan, Pennsylvania State Univ., USA

Session Chair: Sander Stuijk, TU Eindhoven, The Netherlands

**[11:30 – 12:30] Technical Session 3: “TODO”**

Each Talk Slot is of 20 Mins. (18 mins. Presentation + 2 mins. Q&A)

Session Chair: Sherief Reda, Brown University, USA

Talk 1 – Multiprocessor Scheduling of an SDF Graph with Library Tasks Considering the Worst Case Contention Delay

Authors: Hanwoong Jung, Hyunok Oh and Soonhoi Ha

Talk 2 – Temporal Analysis of Static Priority Preemptive Scheduled Cyclic Streaming Applications using CSDF Models

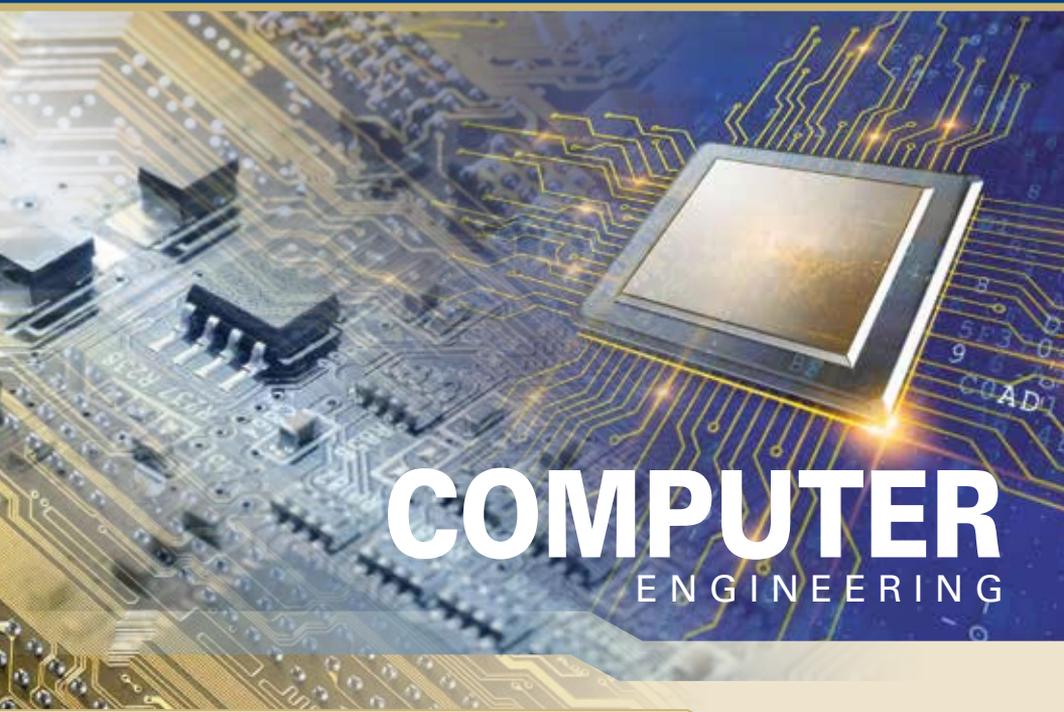
Authors: Philip Kurtin and Marco Bekooij

Talk 3 – An Online Overclocking Scheme for Bursty Real-time Tasks and an Evaluation of its Thermal Impact

Authors: Björn Forsberg, Kai Lampka and Vasileios Spiliopoulos

**[12:30 – 12:45] Closing and Best Paper Award Ceremony**

**[12:45 – 13:15] Poster Discussion**



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## The Swanson School of Engineering and the Computer Engineering program

are proud to sponsor Embedded Systems Week  
in Pittsburgh October 2-7, 2016

**C**omputer Engineering at the University of Pittsburgh is a joint program between the Department of Electrical and Computer Engineering in the Swanson School of Engineering, and the Computer Science Department in the Dietrich School of Arts

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# NOTES





Embedded Systems Week

[www.esweek.org](http://www.esweek.org)

October 2-7, 2016  
Pittsburgh, USA



## Call for Papers

- CASES • CODES+ISSS • EMSOFT • IoT Day • Symposia • Workshops • Tutorials •

### About Embedded Systems Week (ESWeek)

ESWeek is the premier event covering all aspects of embedded systems and software. By bringing together three leading conferences (CASES, CODES+ISSS, and EMSOFT), a special IoT Day, several symposia (like ESTIMedia, RSP), and hot-topic workshops and tutorials, ESWeek presents attendees a wide range of topics unveiling the state of the art in embedded systems design and HW/SW architectures.

#### One Registration, three Conferences !

Registered attendees are entitled to attend sessions of all conference CASES, CODES+ISSS, EMSOFT, and the IoT Day. Symposia, workshops and tutorials require separate registration.

#### Abstract Submission:

April 1, 2016

#### Full Paper Submission:

April 8, 2016 (Firm deadline)

#### Workshop & Tutorial Proposals:

April 8, 2016

#### Notification of Final Acceptance:

July 1, 2016

#### Conference:

October 2-7, 2016

### CASES

### International Conference on Compilers, Architecture, and Synthesis for Embedded Systems

CASES is a forum where researchers, developers and practitioners exchange information on the latest advances in compilers and architectures for high performance embedded systems. In addition to our core areas of technical interest including embedded system architectures, compilers and embedded systems software, memory architectures, architectures targeting power, reliability and security, and emerging application domains, we especially encourage papers that address architectural synthesis and compiler techniques for heterogeneous and accelerator-rich architectures.

### CODES+ISSS

### International Conference on Hardware/Software Codesign and System Synthesis

The International Conference on Hardware/Software Codesign and System Synthesis is the premier event in system-level design, modeling, analysis, and implementation of modern embedded and cyber-physical systems, from system-level specification and optimization down to system synthesis of multi-processor hardware/software implementations. The conference is a forum bringing together academic research and industrial practice for all aspects related to system-level and hardware/software co-design. High-quality original papers will be accepted for oral presentation followed by interactive poster sessions.

### EMSOFT

### International Conference on Embedded Software

The ACM SIGBED International Conference on Embedded Software (EMSOFT) brings together researchers and developers from academia, industry, and government to advance the science, engineering, and technology of embedded software development. Since 2001, EMSOFT has been the premier venue for cutting-edge research in the design and analysis of software that interacts with physical processes, with a long-standing tradition for results on cyber-physical systems, which compose computation, networking, and physical dynamics.

### IoT Day

### Internet of Things: A Holistic Perspective

(IoT Day is part of CODES+ISSS)

Recent advances have led to a vision of a future Internet that connects diverse physical entities, ranging from commonplace household appliances to smart city infrastructure. This Internet of Things brings challenges in research areas including cyber-physical systems, networked sensing, wireless networking, and cloud computing. The IoT Day is designed as a meeting point for researchers with the purpose of exchanging examples of relevant domain challenges and identifying new and exciting interdisciplinary research directions via a combination of contributed and invited papers, talks and panels.

**Paper Process:** This year ESWeek will introduce a two-stage review process in order to further increase quality. Papers passing the first stage of reviews will be asked to revise their work based on reviewer comments within a short time frame of around two weeks. Revised papers will then enter a second stage of reviews to decide on final acceptance. For details, see <http://esweek.org/author-information>

[www.esweek.org](http://www.esweek.org)



# 12TH ACM/IEEE EMBEDDED SYSTEMS WEEK



**ESWEEK 2016**  
**OCTOBER 2-7, 2016**  
**PITTSBURGH, PA, USA**